

**JP-8 SERVICE NOTES**

*Second Edition*  
December.1982

This Notes makes First Edition obsolete and consists of two parts:

**Part 1 Previous First Edition . . . . pp.1-31**

**Part 2 Mainly applicable to JP-8 units with Serial Numbers**

**171700 and above . . . . pp.32-46**

**Parts List Change . . . . p.47**

**Appendix . . . . pp.48-50**

**BEFORE READING**

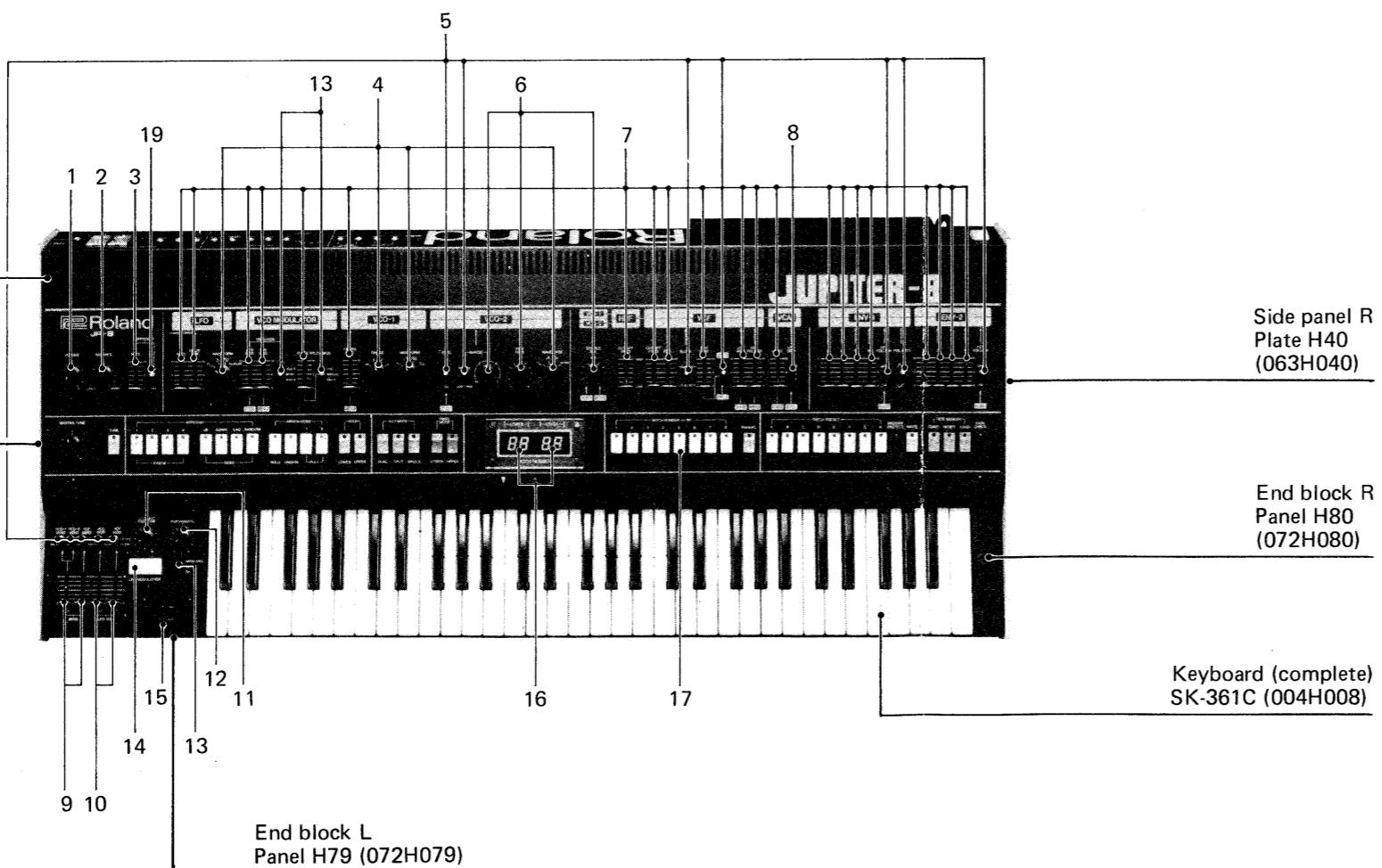
**PLEASE CHECK FOR CHANGE INFORMATION**

**AND CONTENTS AT PAGES 32 AND 33**

**OF THIS NOTES.**

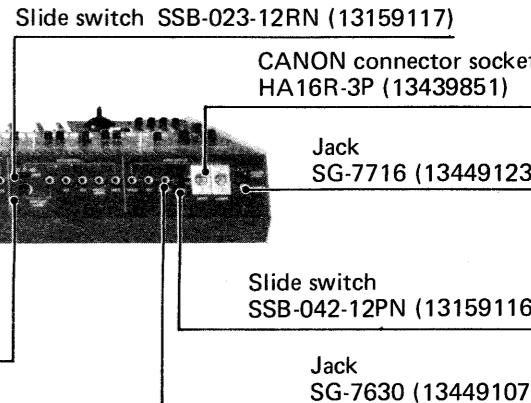
**SPECIFICATIONS**

Keyboard:	61 Note, 5 Octaves	Arpeggio	
VCO		Rate:	1 - 20Hz
VCO-2 Fine Tune Range:	±50 Cents	Audio Outputs	
VCF		Upper:	0dBm, 600 Ohm, Balanced
Slope:	12/Octave, 24/Octave	Lower:	0dBm/-20dBm, 1k Ohm, Unbalanced
Key Follow:	0 - 120%	Highest Note Output	
ENV		CV:	0 - 5V
ENV-1, 2		Gate:	Off - 0V, On - +15V
Attack Time:	1ms - 5s	Dimensions:	1063(W) x 485(D) x 120(H)mm
Decay Time:	1ms - 10s	Weight:	22kg
Sustain Level:	0 - 100%	Power Consumption:	90W
Release Time:	1ms - 10s		
LFO			
Rate:	0.05 - 40Hz		
Delay Time:	0 - 4s		
Master Tunable Range:	±50%		



Power switch  
2Wi x II (13149103) 115V  
2Wi II (13149104) 220V

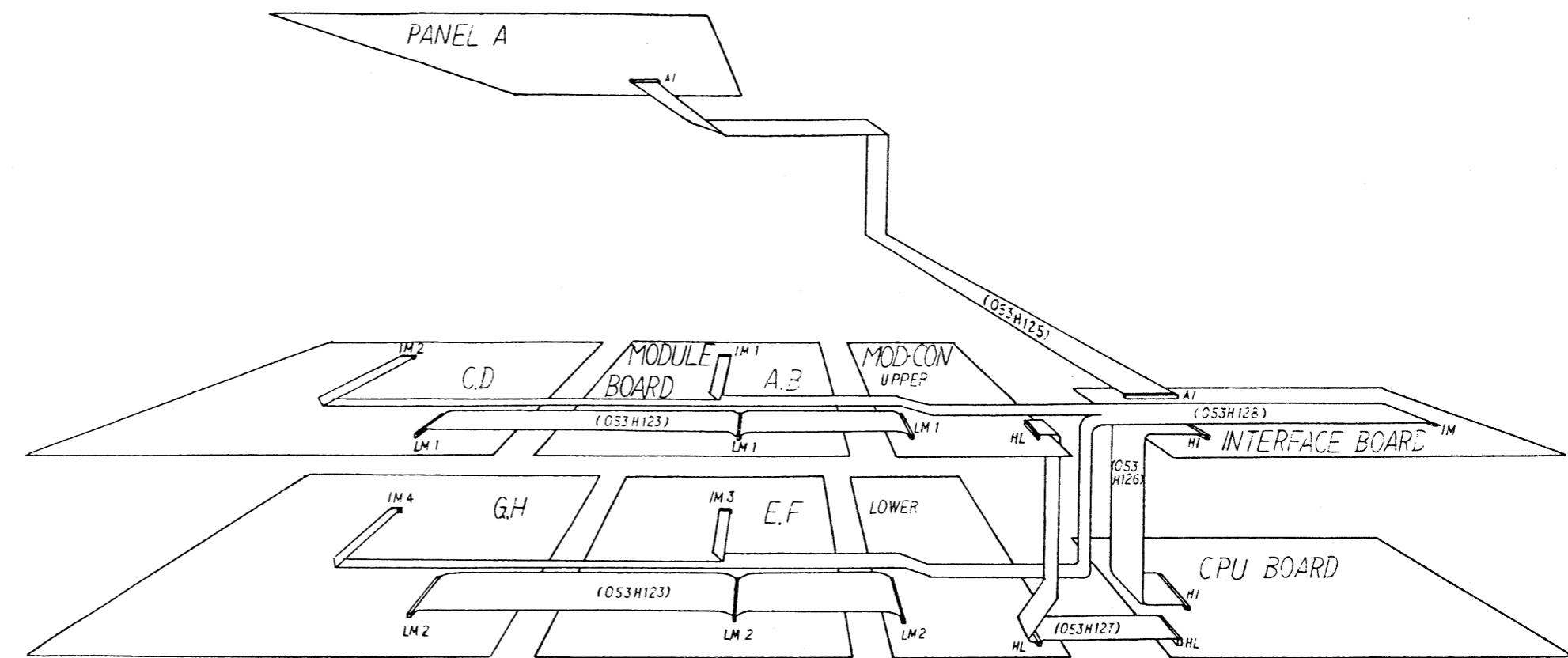
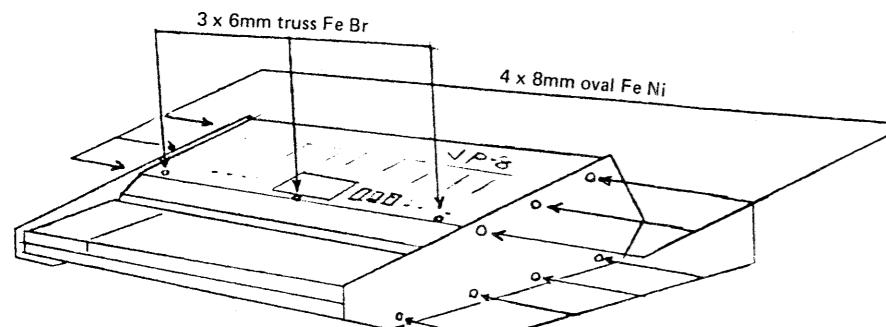
Slide switch  
SSB-022-12RN (13159118)

**JP-8 PANEL PARTS LIST**

1	Pot.	GM70R-K20B54 (50KB x 2) (13219812)
2	Pot.	GM70R-K20AC54 (50KA, C) (13219811)
3	Pot.	LFE9R-C16A55 (500KA) (13339414)
4	Switch	SRM1034-K15 (13119301)
5	Switch	SLE622-18PS (13139137)
6	Pot.	VM10R-K20B14 (10KB) (13219225)
7	Pot.	LFE9R-C16B14 (10KB) (13339415)
8	Switch	SQPR-24-12P (13159503)
9	Pot.	LFE9R-C16B54 (50KB) (13339413)
10	Pot.	MFE9R-C16B54 (50KB x 2) (13359302)
11	Pot.	VM10R-K20A55 (500KA) (13219231)
12	Pot.	VM10R-K20C54 (50KC) (13219243)
13	Switch	SLE623-18P (13139135)
14	Switch w/key top	KEH10003 (13129717) See Parts List for Key top and Switch
15	Bender assy	PB-4 (029-022)
16	Cover LED	H80 (065H080) LN526RA (15029404)
17	Switch	KHC11901 (13169601)
	Buttons	
No.1, 38		RED (016H018)
No.2-5, No.34-37		ORANGE (016H012)
No.6-9, No.30-33		YELLOW (016H017)
No.10-13, No.21-28		WHITE (016H010)
No.14, 15, 29		GREEN (016H014)
No.16-18, No.39-41		BLUE (016H013)
No.19, 20		DARK BLUE (016H011)
18	Pot.	VM10A-K15B54 (50KB CT) (13229131)
19	Switch	SLE-622-18P (13139136)
	All rotary knobs	No.68 (016-078)
	All slider knobs	H4 (016H004)

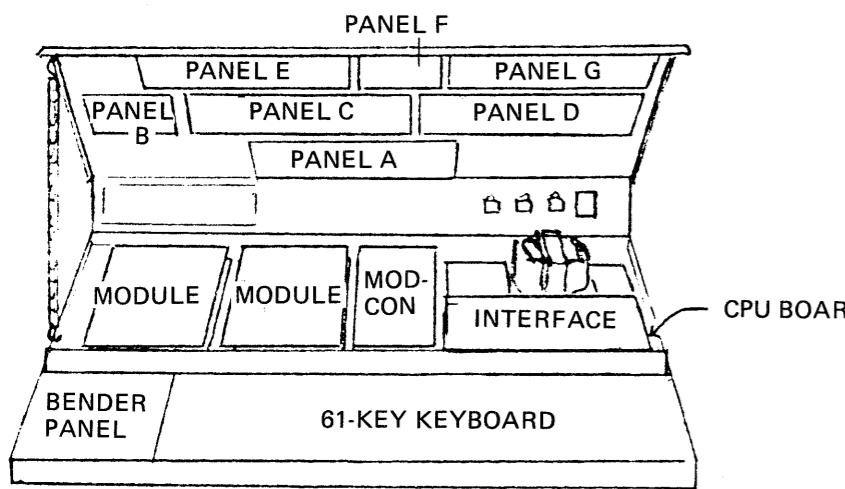
## DISASSEMBLY

Remove screws ①, ② and ③.



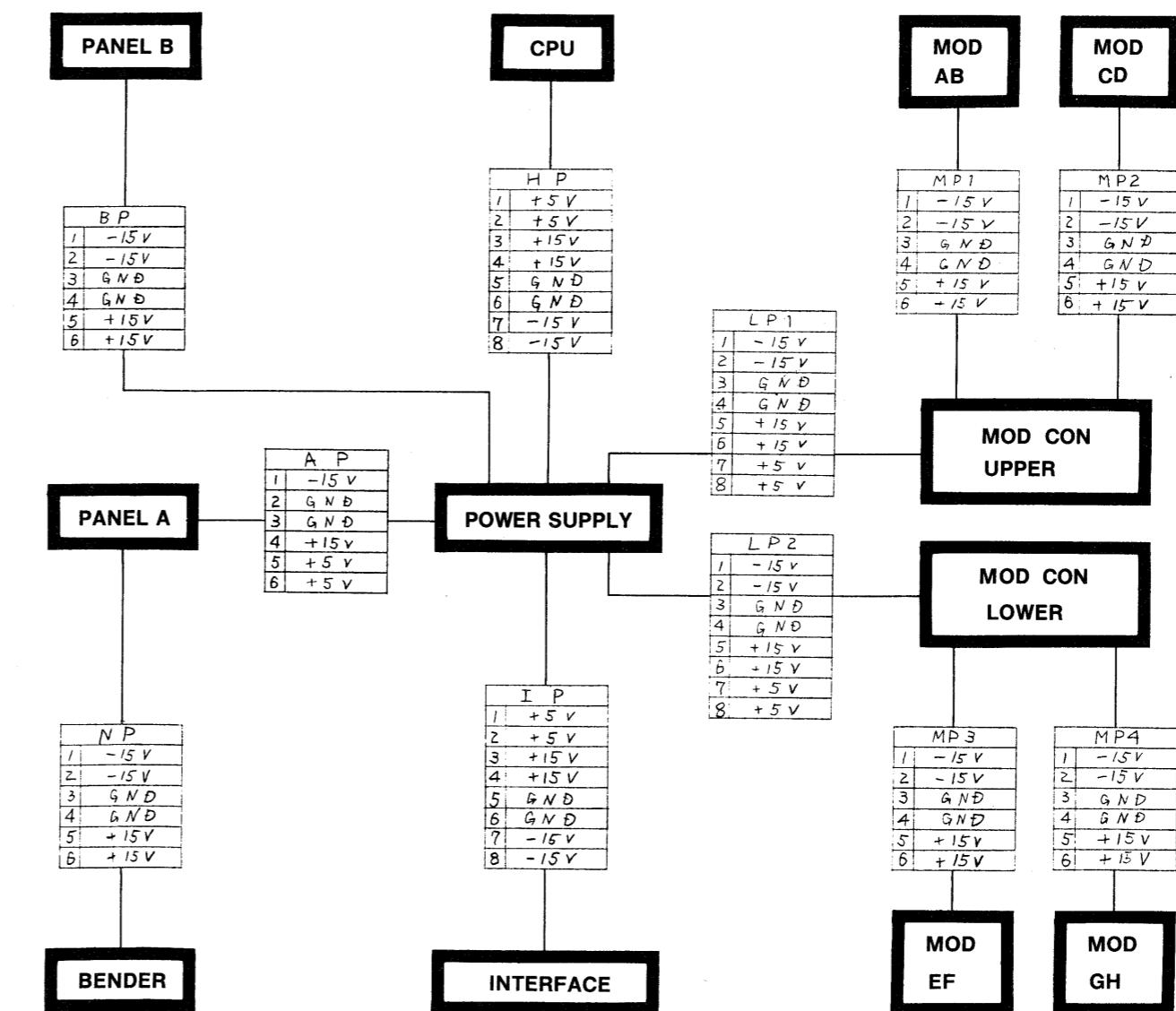
## NOTE:

Preparation of a stay and a prop is recommended for a stable top panel rest.



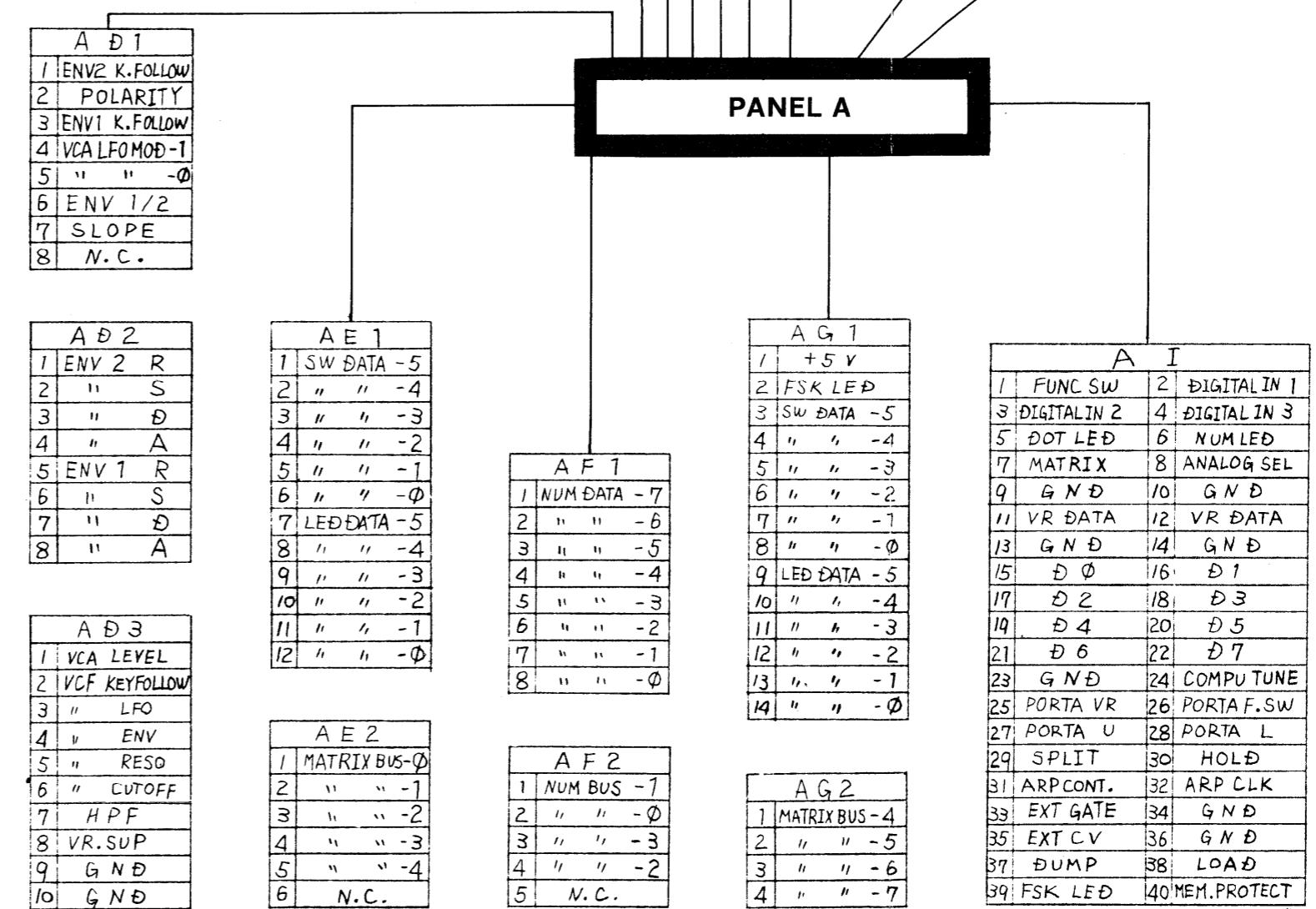
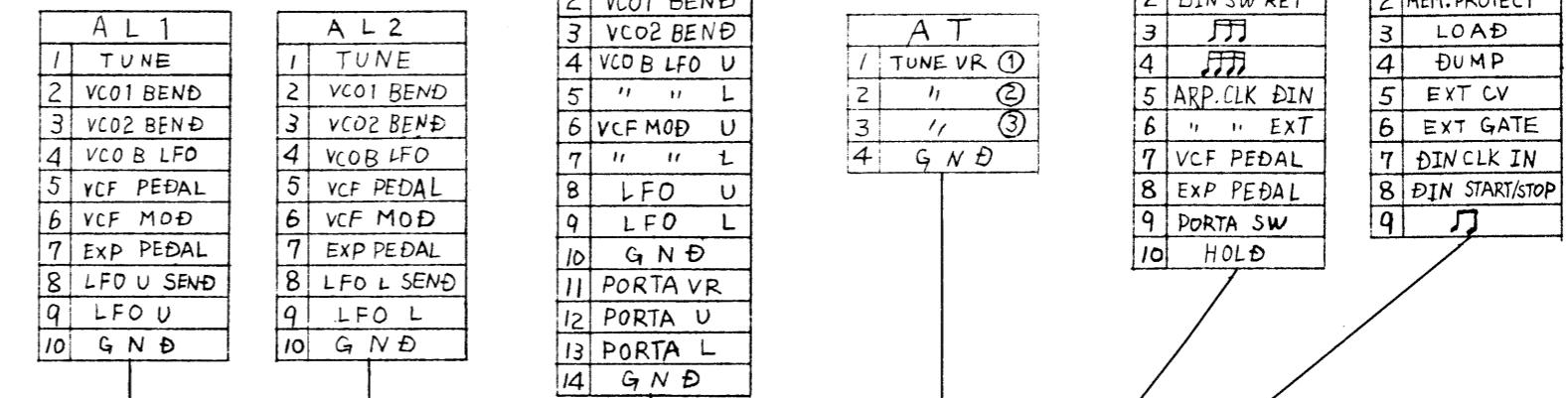
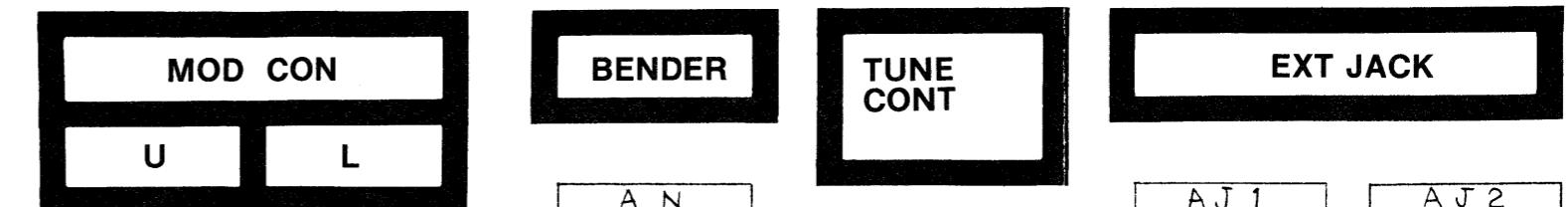
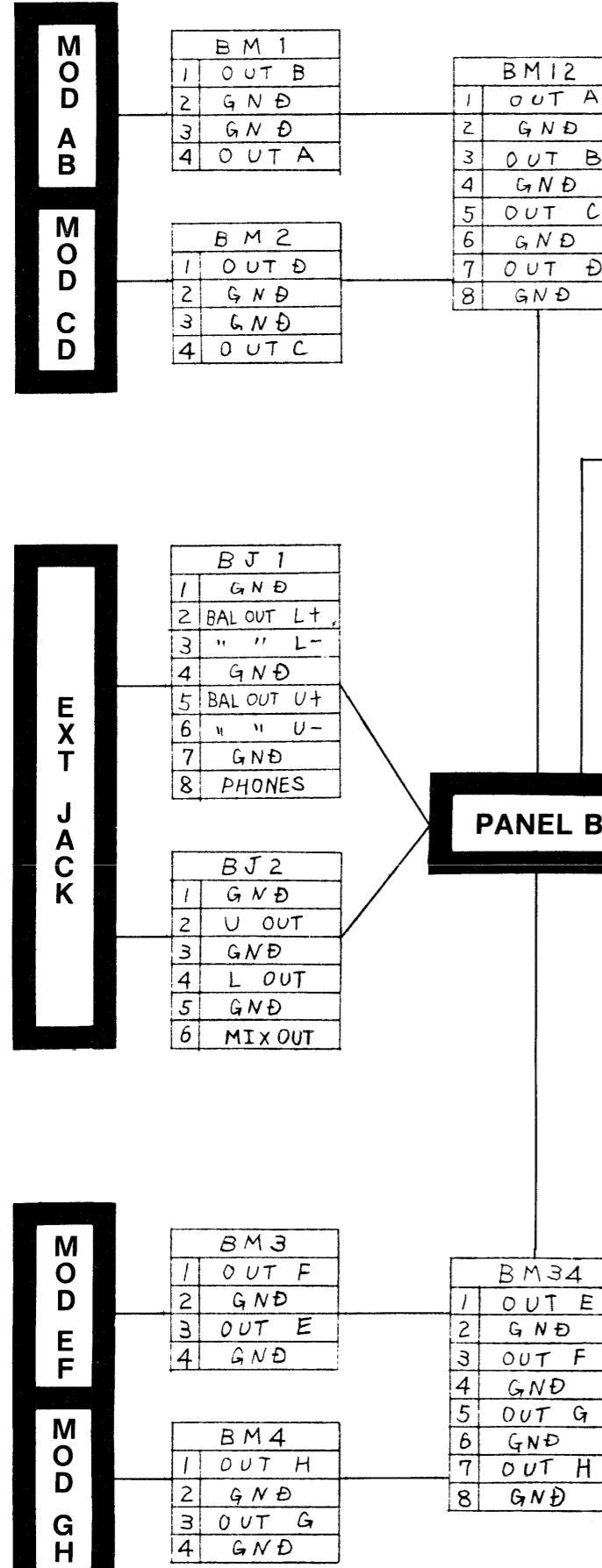
## PRECAUTIONS

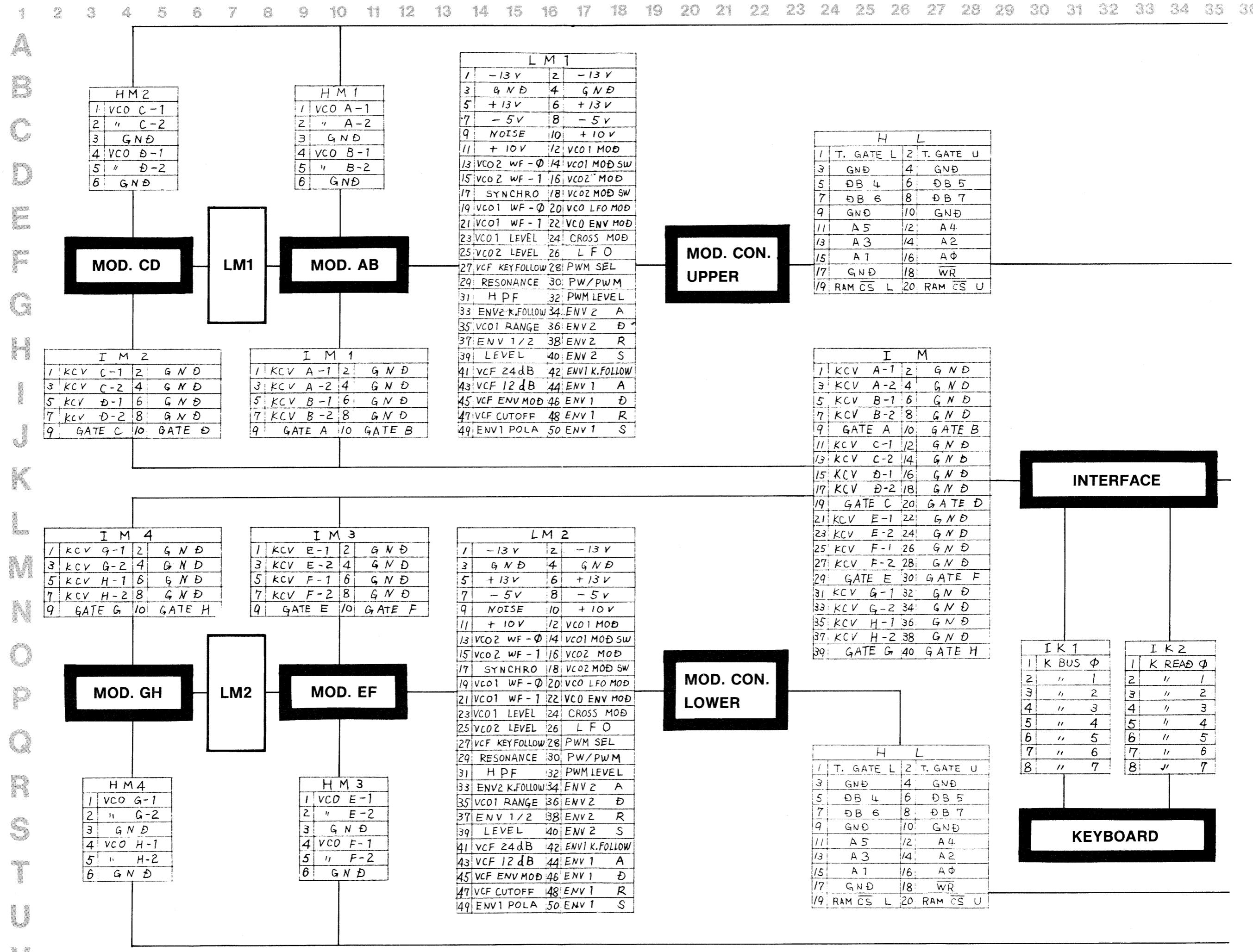
1. Do not pinch flat cables in the pcbs when closing panel assemblies. Prongs on PCBs will pierce humped cable, causing circuits to malfunction. Stretch rolling cable out.
2. Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, PCBs are temperature-sensitive.



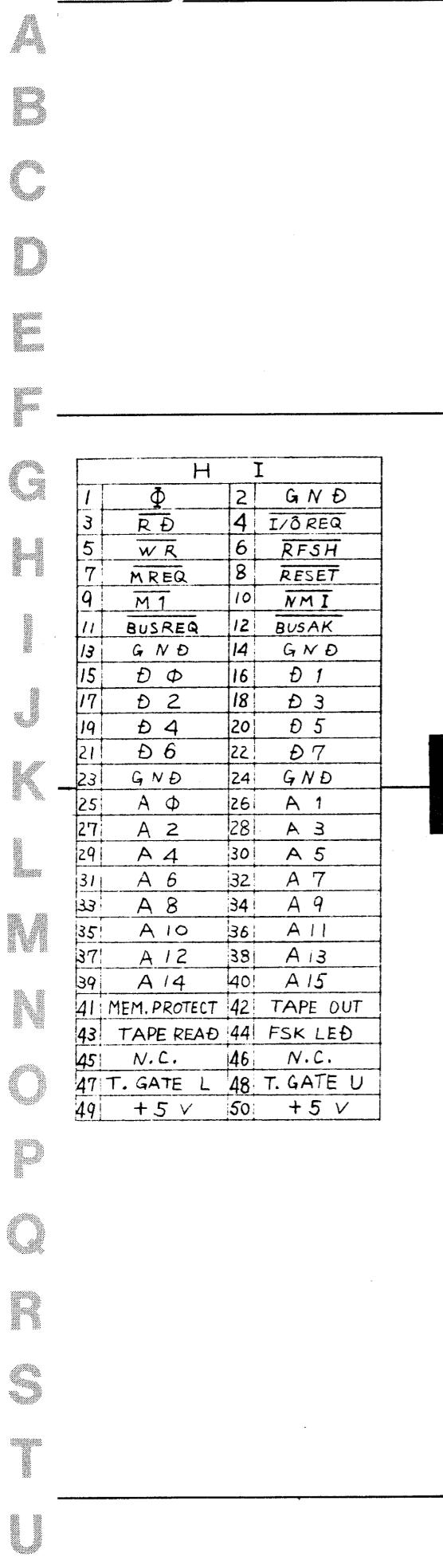
OCT.10, 1981

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

A  
B  
C  
D  
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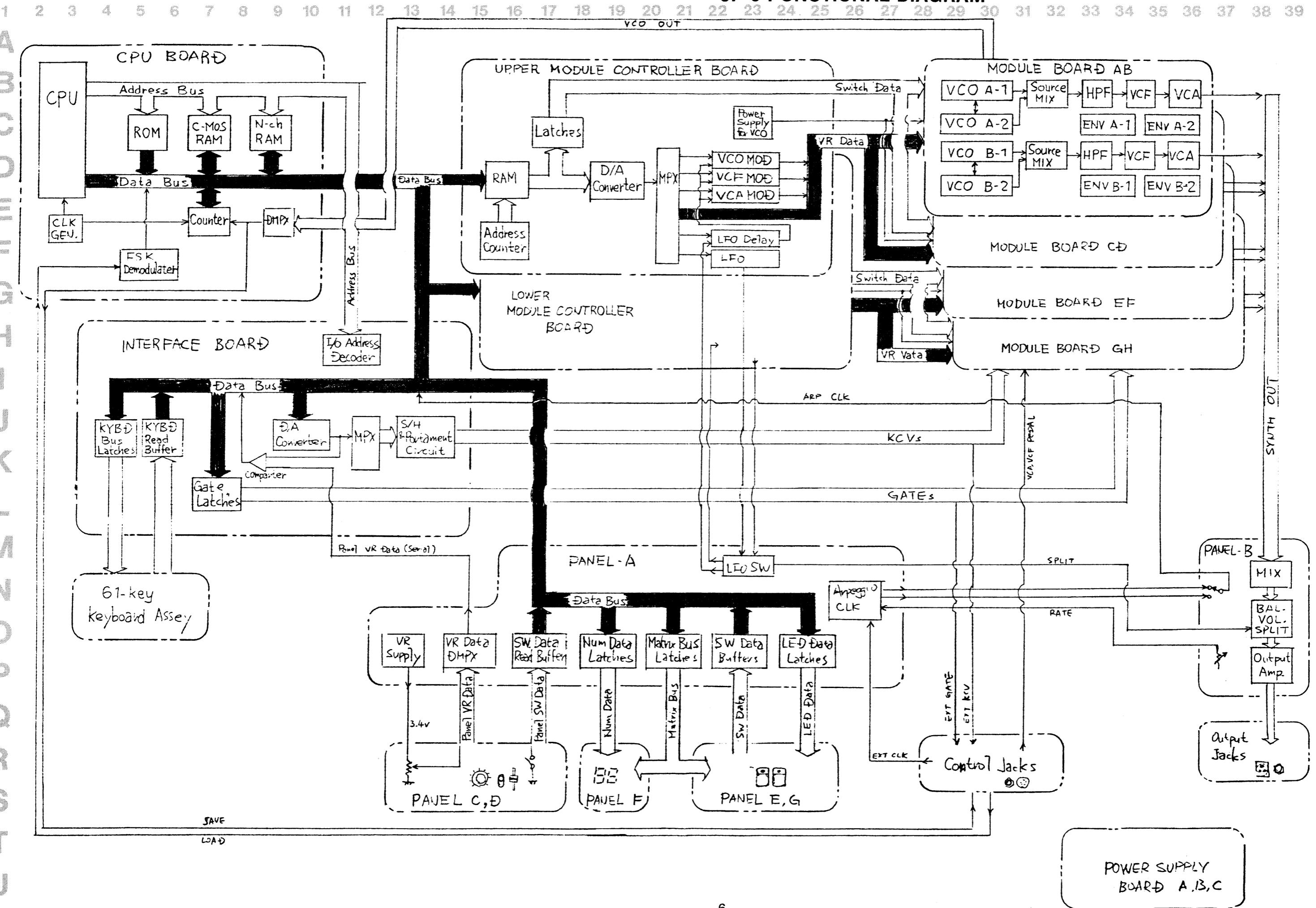
1 2 3 4 5 6 7 8 9 10 11 12 13

**CPU BOARD**

H M 12	
1	VCO A-1
2	" A-2
3	GND
4	VCO B-1
5	" B-2
6	GND
7	VCO C-1
8	" C-2
9	GND
10	VCO D-1
11	" D-2
12	GND

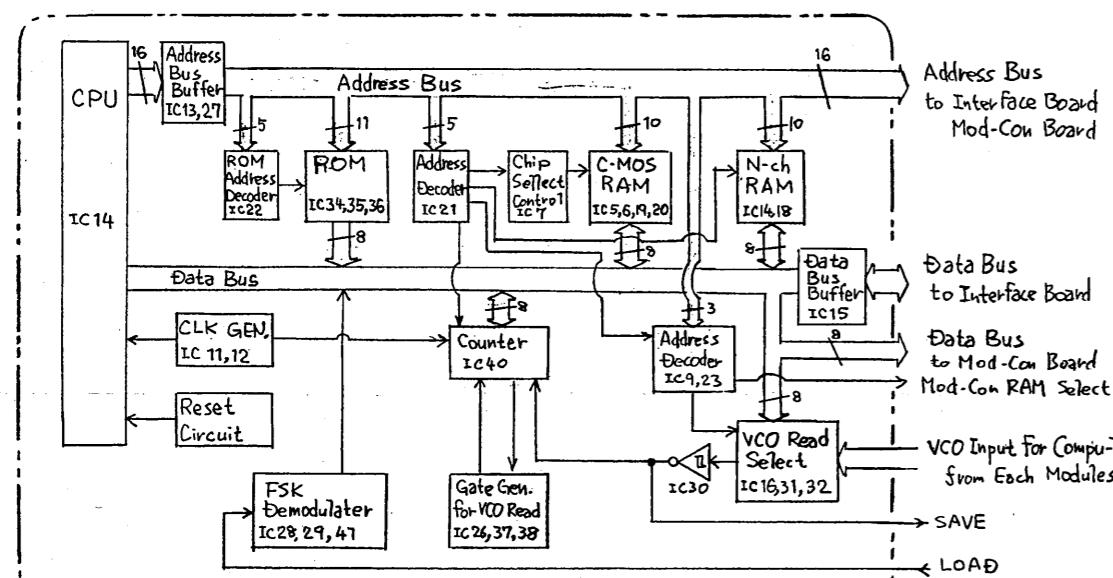
H I	
1	Φ
3	R D
5	WR
7	MREQ
9	M1
11	BUSREQ
13	GND
15	DΦ
17	D2
19	D4
21	D6
23	GND
25	AΦ
27	A2
29	A4
31	A6
33	A8
35	A10
37	A12
39	A14
41	MEM.PROTECT
43	TAPE READ
45	N.C.
47	T.GATE L
49	+5 V
50	+5 V
51	TAPE OUT
52	FSK LED
54	N.C.
56	T.GATE U

H M 34	
1	VCO E-1
2	" E-2
3	GND
4	VCO F-1
5	" F-2
6	GND
7	VCO G-1
8	" G-2
9	GND
10	VCO H-1
11	" H-2
12	GND

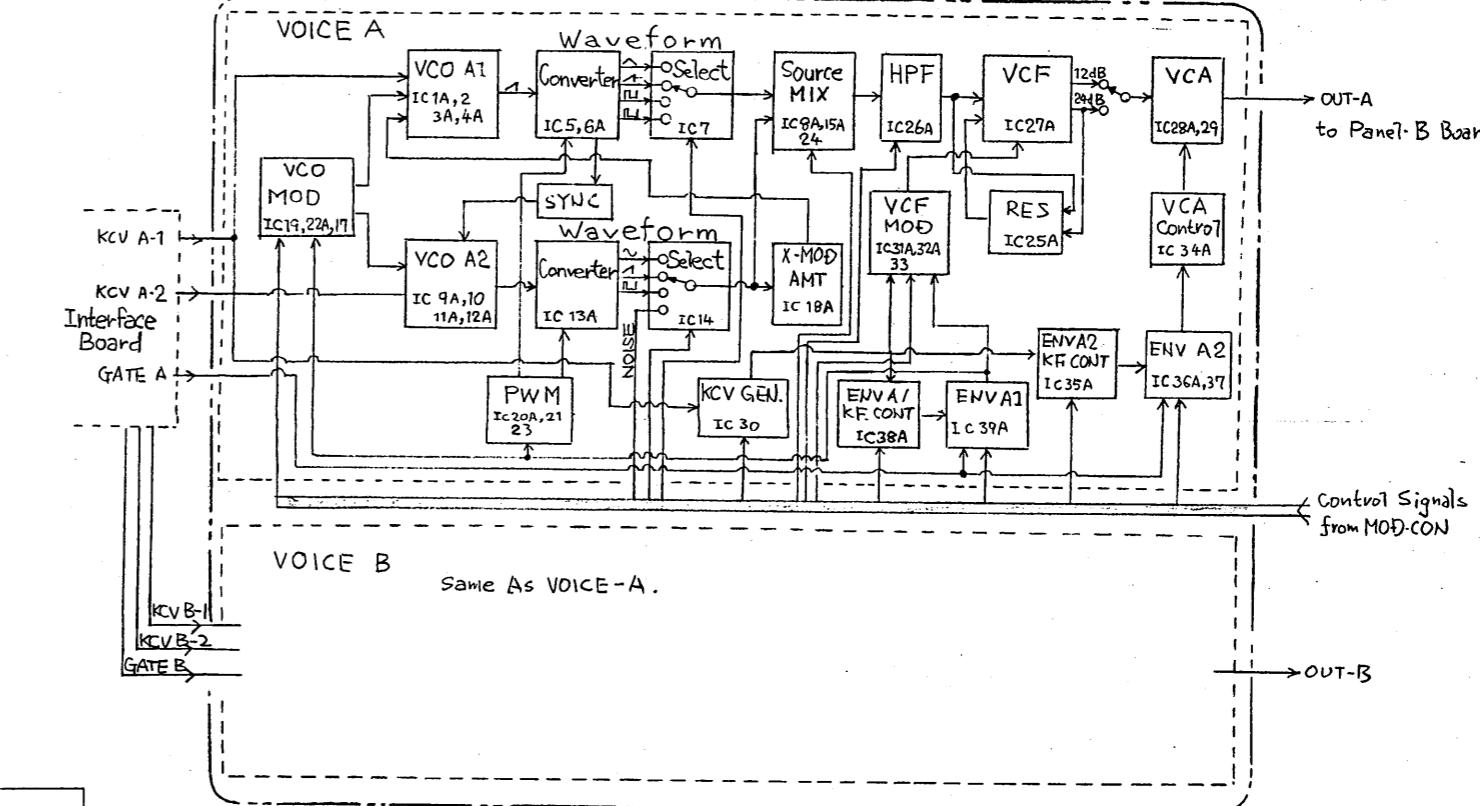
JP-8  
JP-8 FUNCTIONAL DIAGRAM

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49

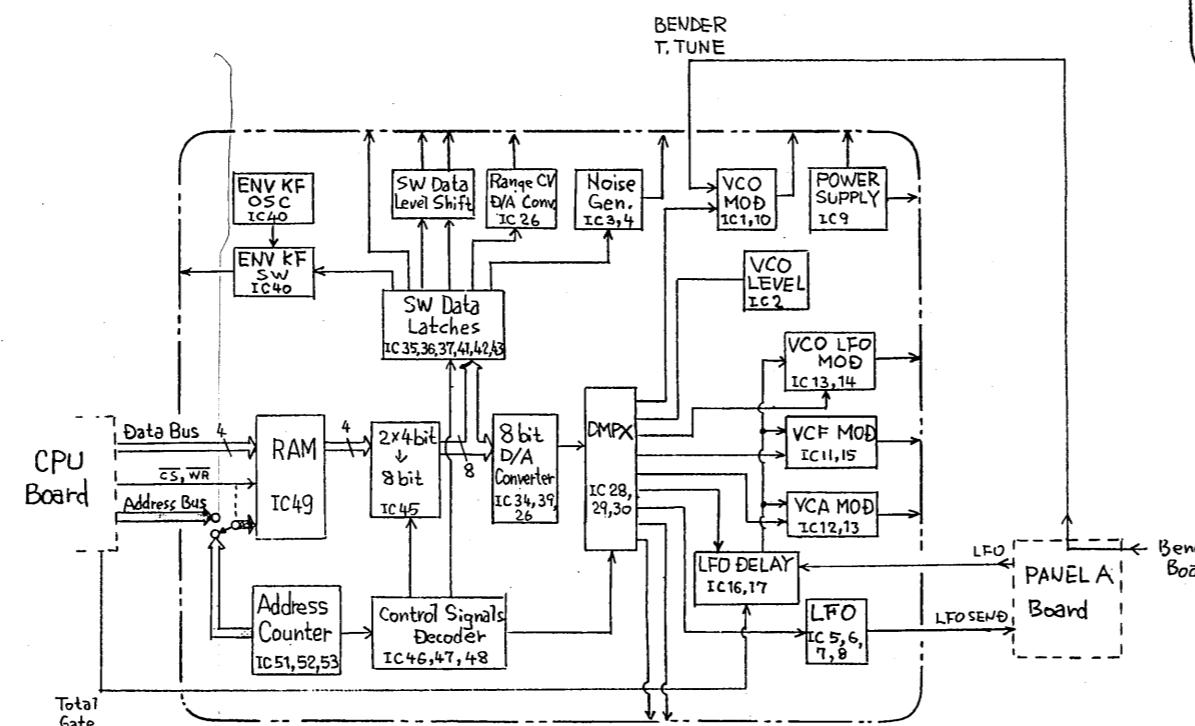
A  
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G  
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J  
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L  
M  
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O  
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Q  
R  
S  
T  
U  
V  
W  
X  
Y  
Z



CPU BOARD BLOCK DIAGRAM

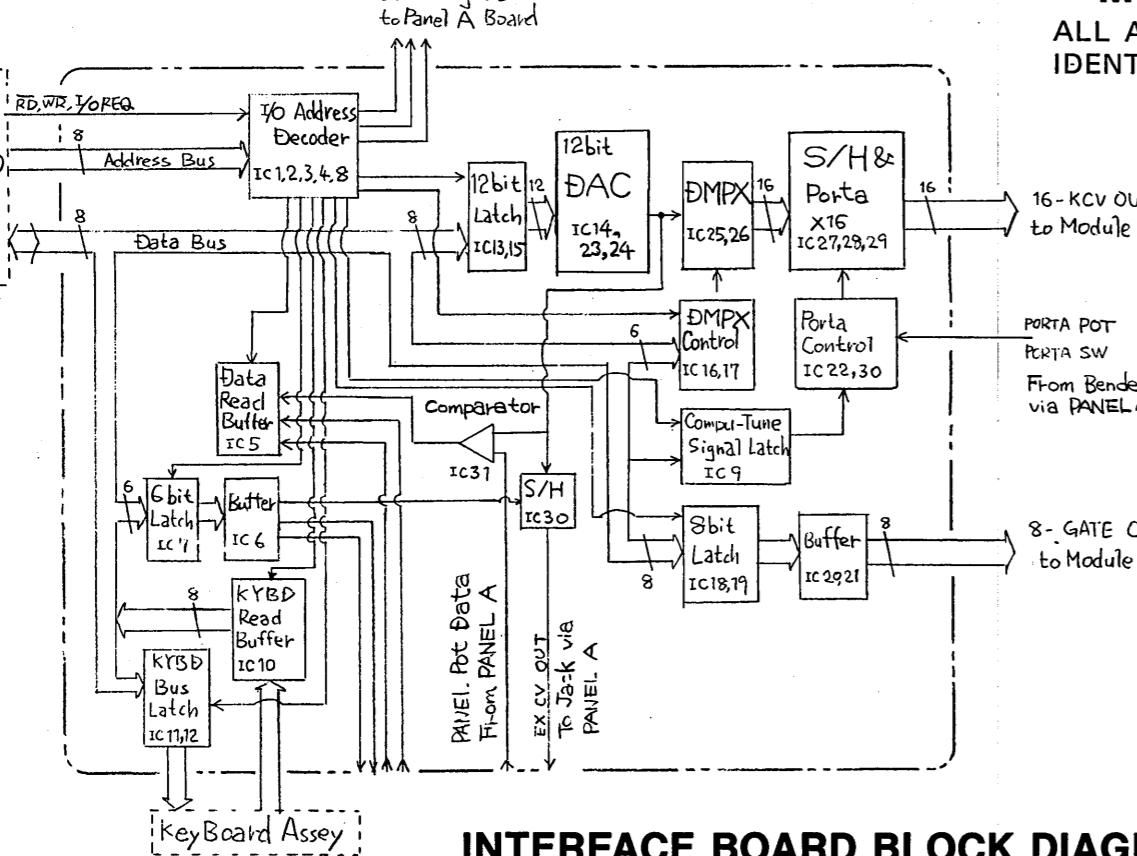


MODULE BOARD BLOCK DIAGRAM

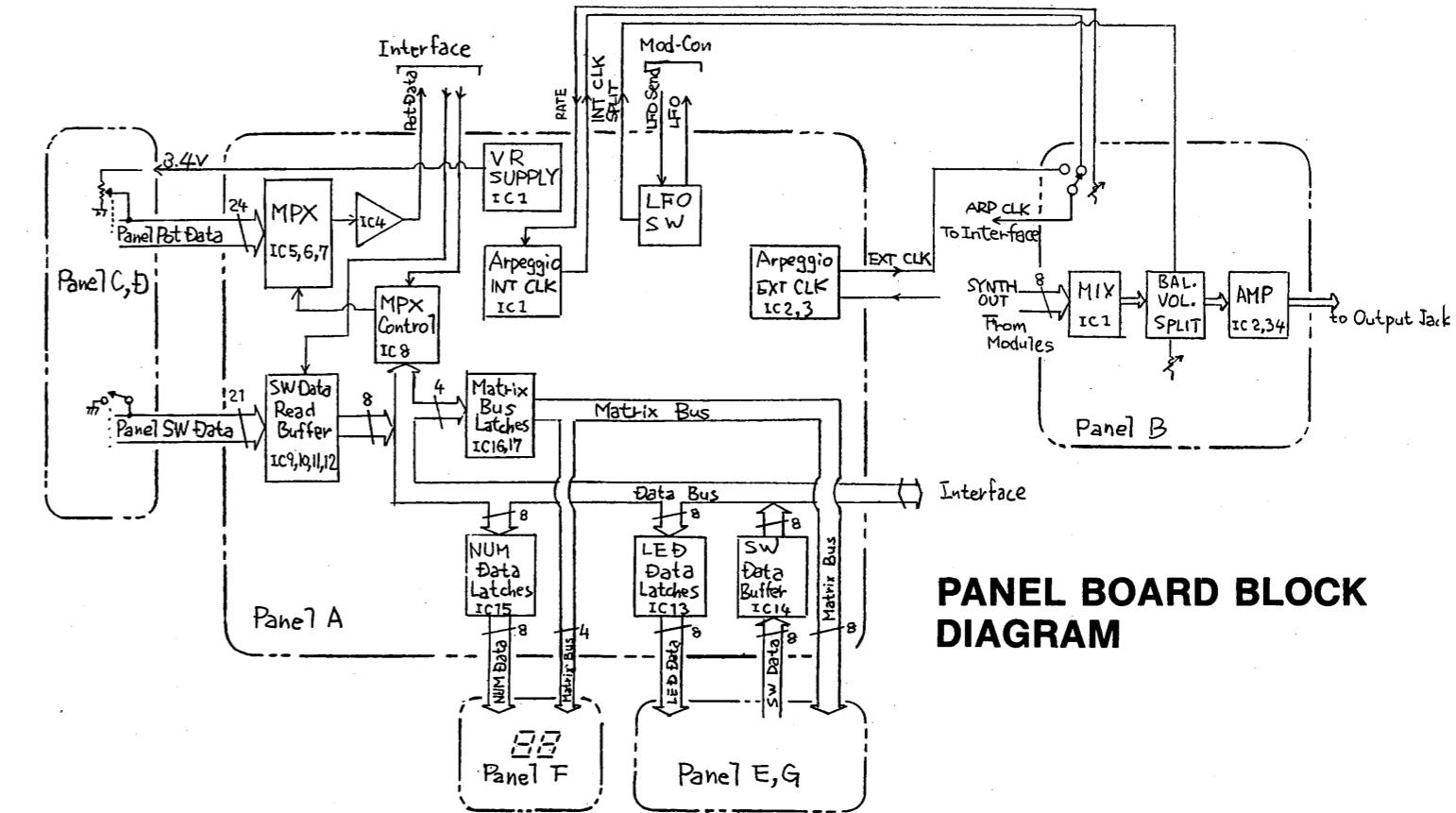


MOD-CON BOARD BLOCK DIAGRAM

ALL ARROWS HAVING NO DESTINATION IDENTIFIER CONNECT TO MODULE BOARD.



INTERFACE BOARD BLOCK DIAGRAM



PANEL BOARD BLOCK DIAGRAM

A  
B  
C

**D  
E  
F  
G**

10

- J  
K

M

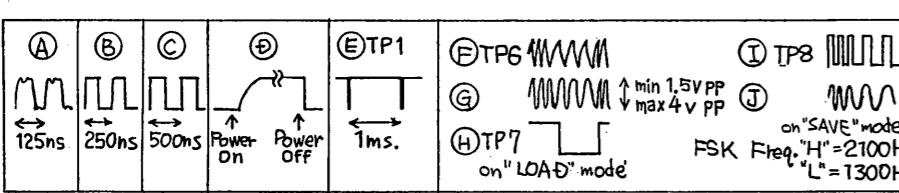
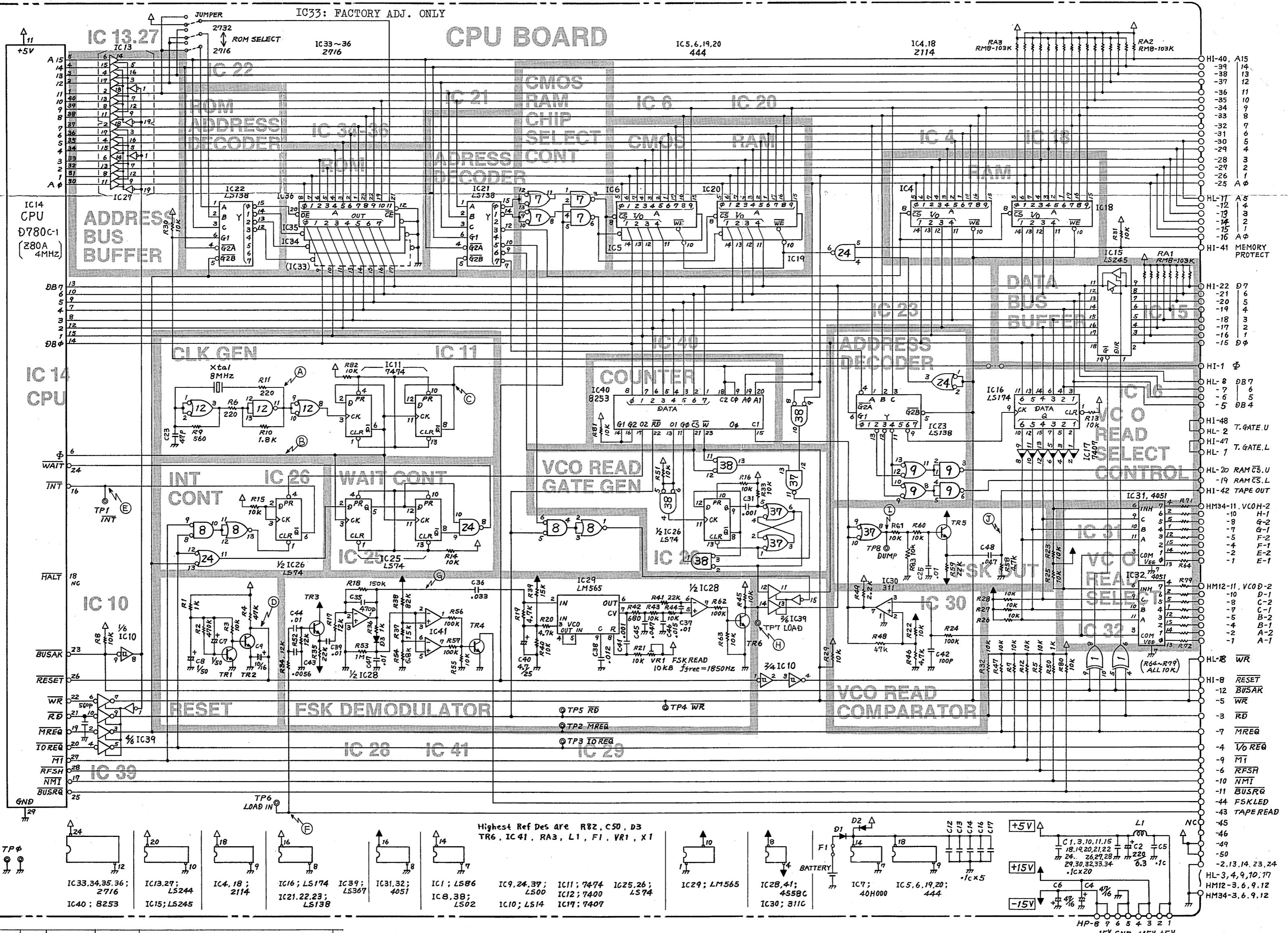
N  
O  
P  
Q

R  
S  
T

U  
V

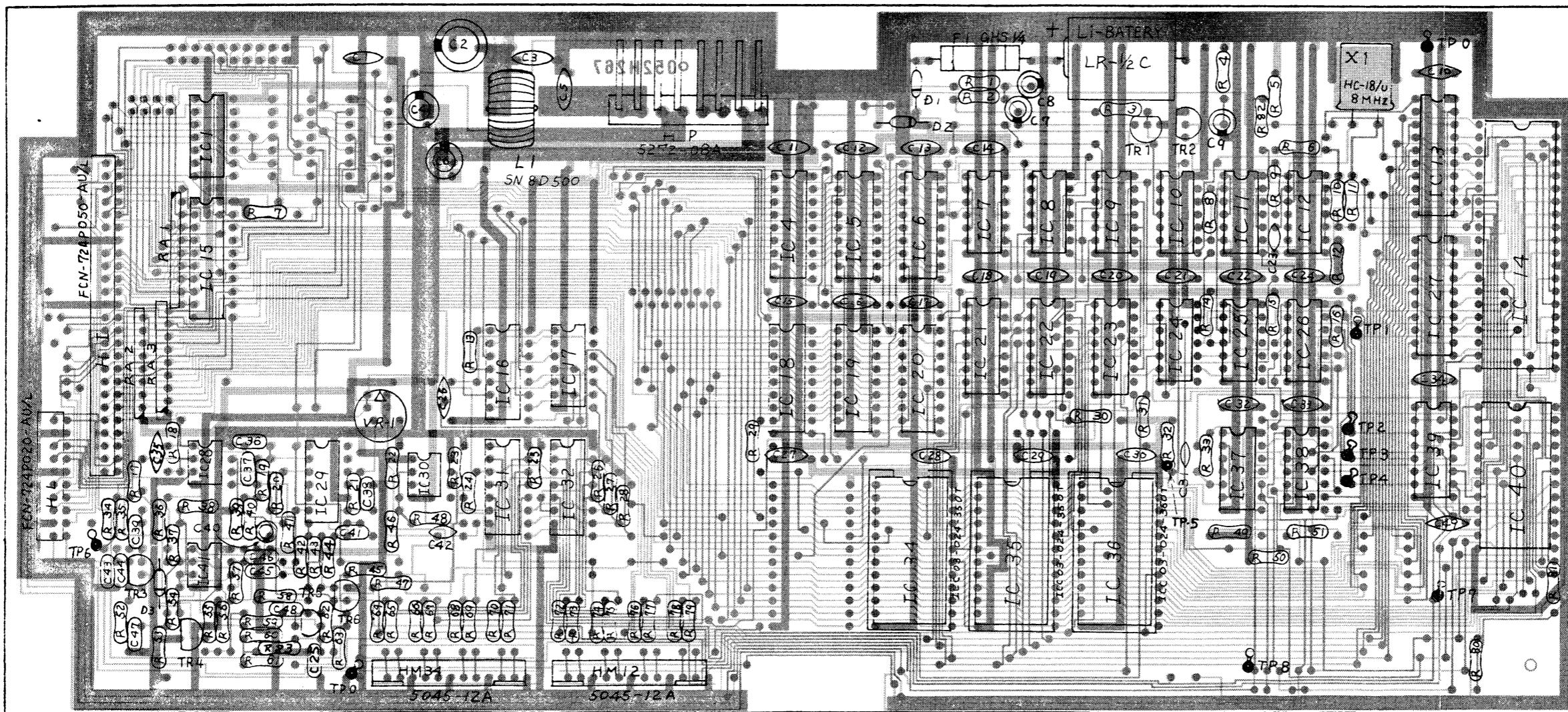
W

X  
Y  
Z



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

CPU BOARD OPH121(149H121)(pcb 052H26)



 R 25 J

2SC1815-GR

LC-2

△ SR 19R

IS247

RM8-103A

Refer to Page 38 for

## CPU CHANGE INFORMATION

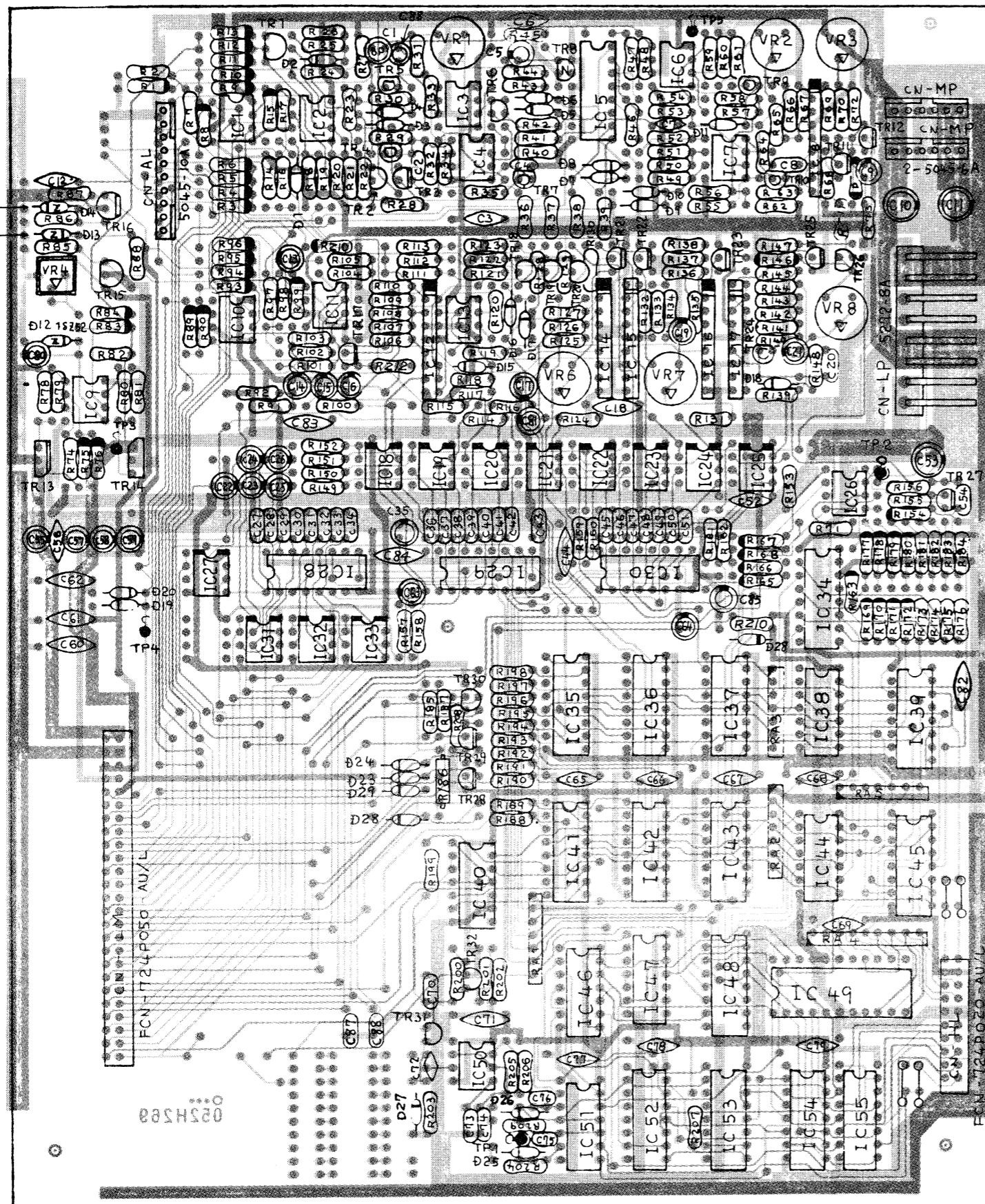
## CAUTIONS ON MODULE CONTROLLER BOARD REPLACEMENT

## RAM (MOD CON BOARD) REPLACEMENT

CPU BOARD WILL BE AFFECTED BY THESE REPLACEMENTS

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

A B C D E F G H I J K L M O P R S T V

**MODULE CONTROLLER**

OPH123(149H123) (pcb 052H269)

SN 090600-192099

## REFER TO PAGES

49-50 for SN up to 090599

36-37 for SN 202100-up

37-38 for PCB or RAM REPLACEMENT

selected on current leakage  
white dot

R 50J  
1/4w carbon R25  
1/4w metal film CRB25FX  
D resistor ERS-C33 G561

1S2473  
zener diode

5R19R  
ET-6P

2SA1015-GR  
2SC1815-GR

2SC945 selected for Noise

2SK30A-GR  
2SK117-GR

2SB605  
2SD571

BA662

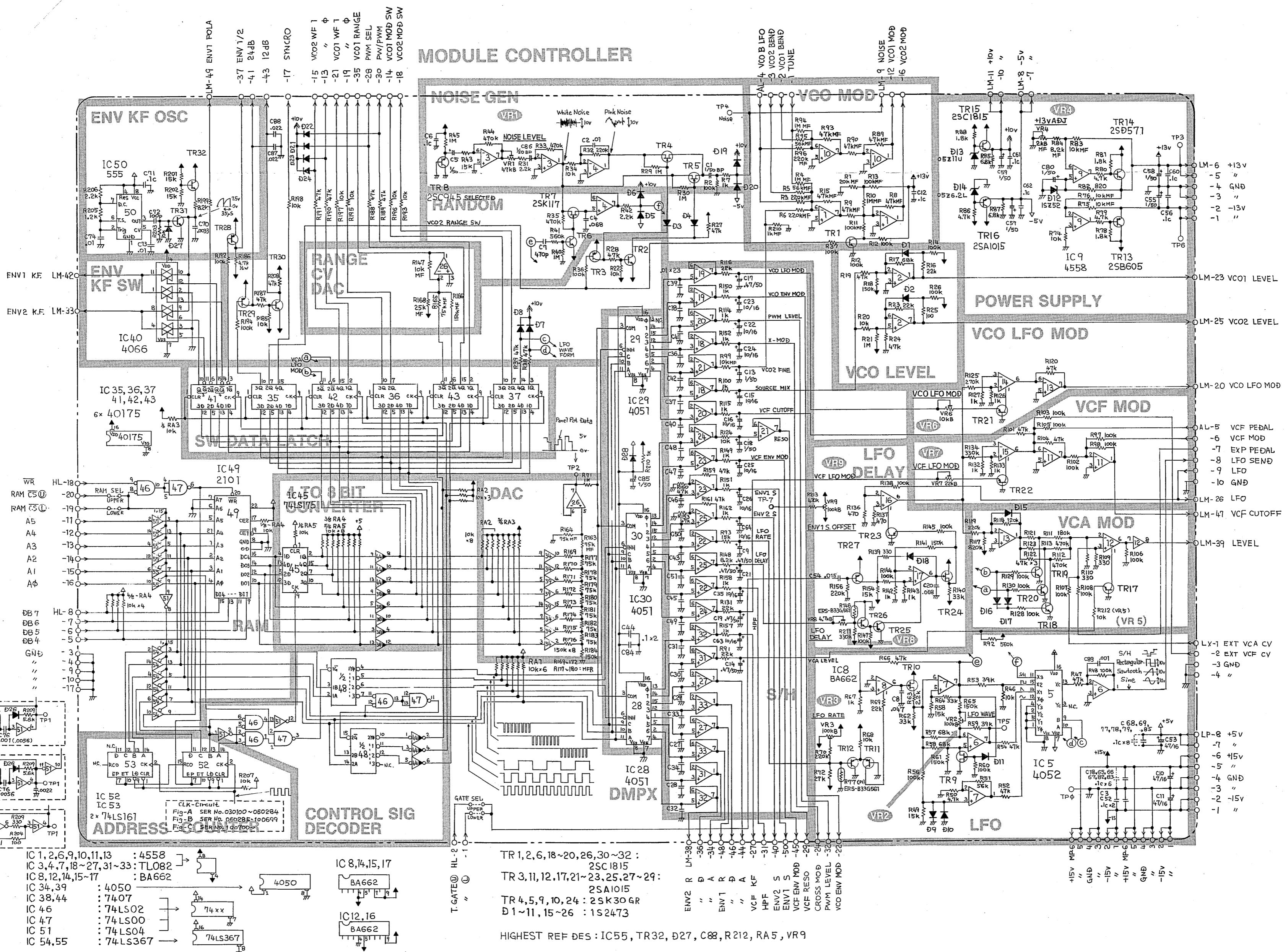
Resistor array

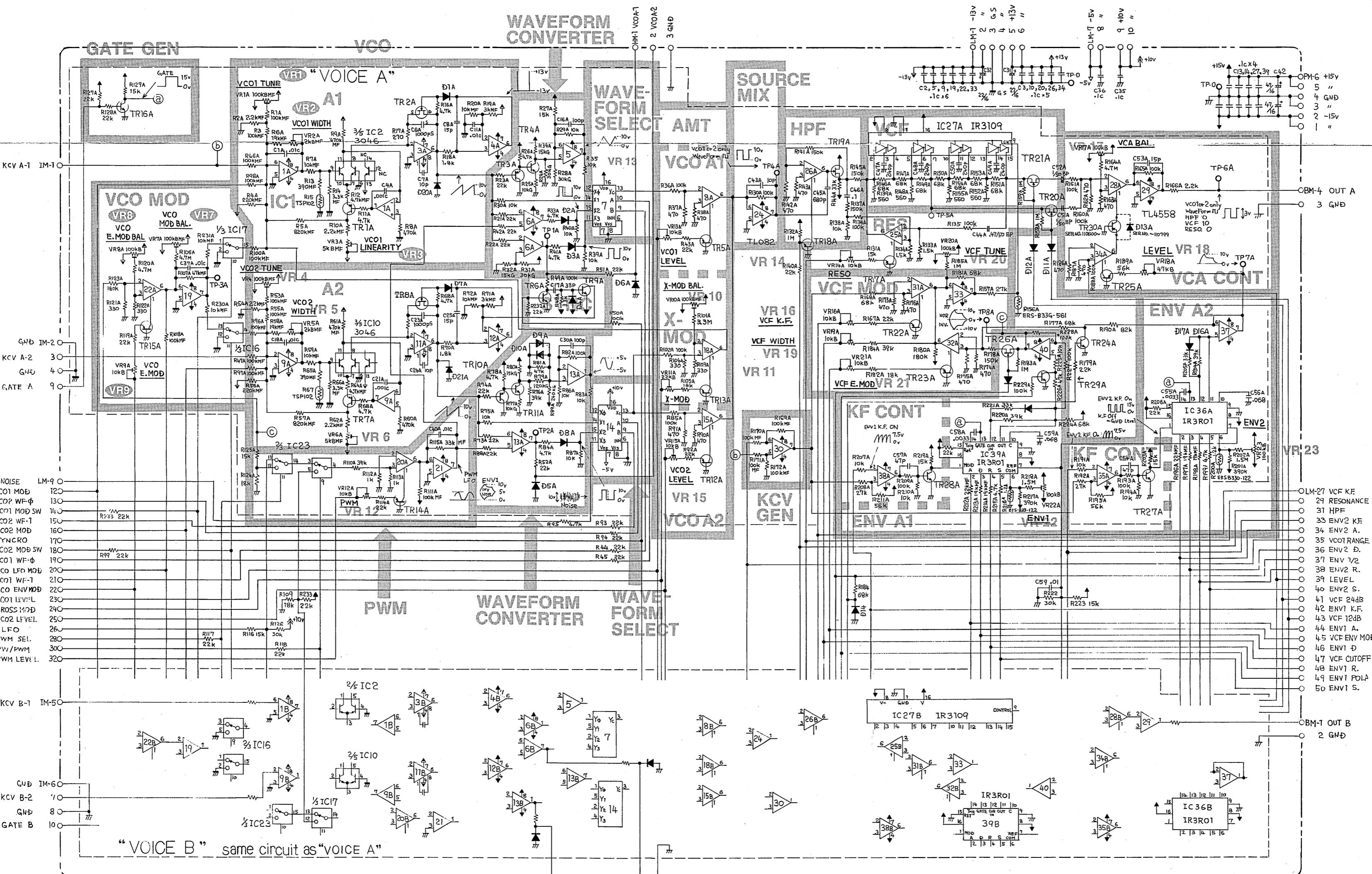
BA662A selected on  
offset

bi-polar

test point LC-2-S

A  
B  
C  
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Z



MODULE BOARD CIRCUIT DIAGRAM  
MODULE BOARDA  
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G  
H  
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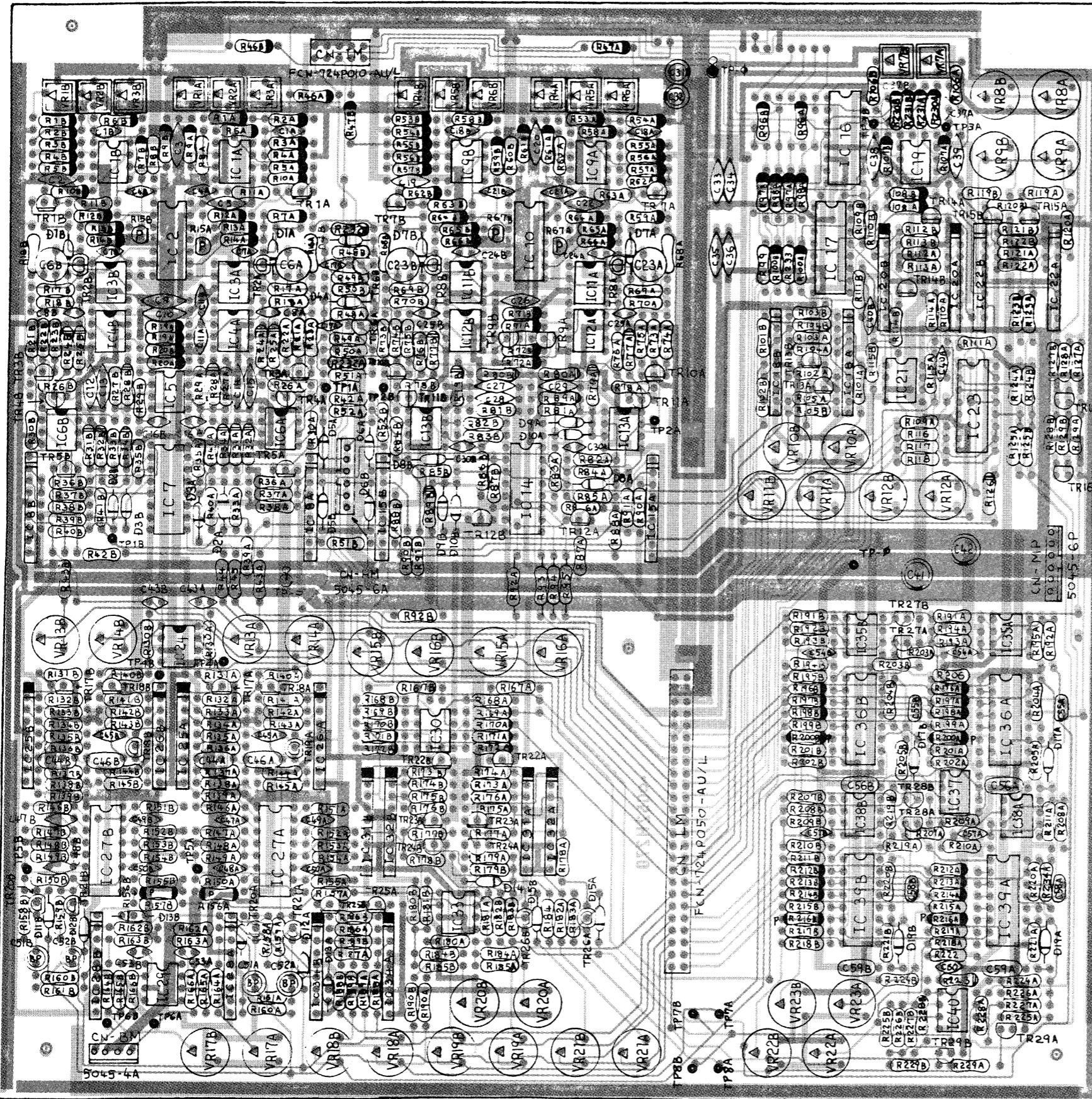
IC1A,1B,5,9A,9B,19,21,30,33,37,40 : 4558  
 IC2,10 : RC3046  
 IC3A,3B,4A,4B,11A,11B,12A,12B,35A,35B,38A,38B : TL080  
 IC6A,6B,13A,13B,24 : TL082  
 IC7,14 : 4052  
 IC8,8B,15A,15B,18A,18B,20A,20B,22A,22B,25A,  
 25B,26A,26B,28A,28B,31A,31B,32A,32B,34A,34B : BA662  
 IC16,17,23 : 4053  
 IC27A,27B : IR3109  
 IC29 : TL4558 or NJM4659D  
 IC36A,36B,39A,39B : IR3R01

A1 PNP TR : 2SA1015-GR  
 TR 4A,4B,9A,9B,11A,11B : 2SC1552-Y  
 Other NPN TR : 2SC1815-GR  
 TR 2A,2B,9A,9B : NFT10  
 Other FET : 2SK30A-GR  
 All Diode : 1S2473

There are two different GND lines. "||" is not connected to "||" on this PCB.  
 Highest Ref. Des. are IC 40, TR2A, D34B, C60, R220B, VR23B  
 30B 21B

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

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V



**MODULE BOARD**  
**OPH124(149H124)**  
**(pcb 052H270)**

**SEE PAGE 48**  
**For SN up to 090599**

 R25G selected on slew rate  
 TL080 8pcs  
 C82 5pcs

 carbon R25

 metal film RB25FX

 posistekters-C33G561

 posistek TSP102

 2SA1015-GR

 2SC1815-GR

 2SC1752-Y

 2SK30A-GR

 NF510

 1S2473

 BA662

 ET-6P

 A or B  
 selected on VF (gm)  
 replacement should  
 if the existing

Selected on offset  
10 pc's  
white dot

SR19

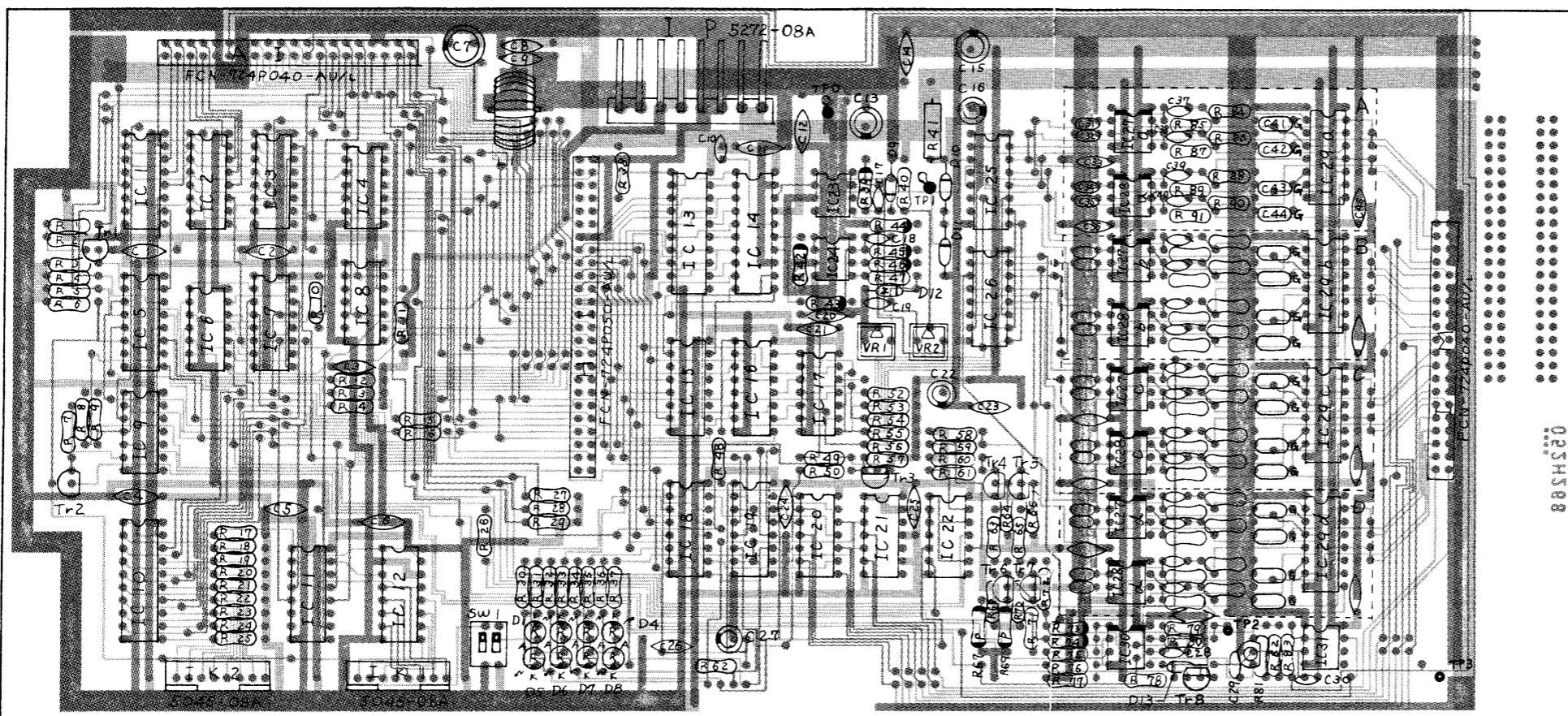
8 test point LC-2S (TP-Φ : GND)

○ polystyrene film

(BP) bi-polar

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 **INTERFACE BOARD** **OPH122(149H122)(rev.052H268)**

A  
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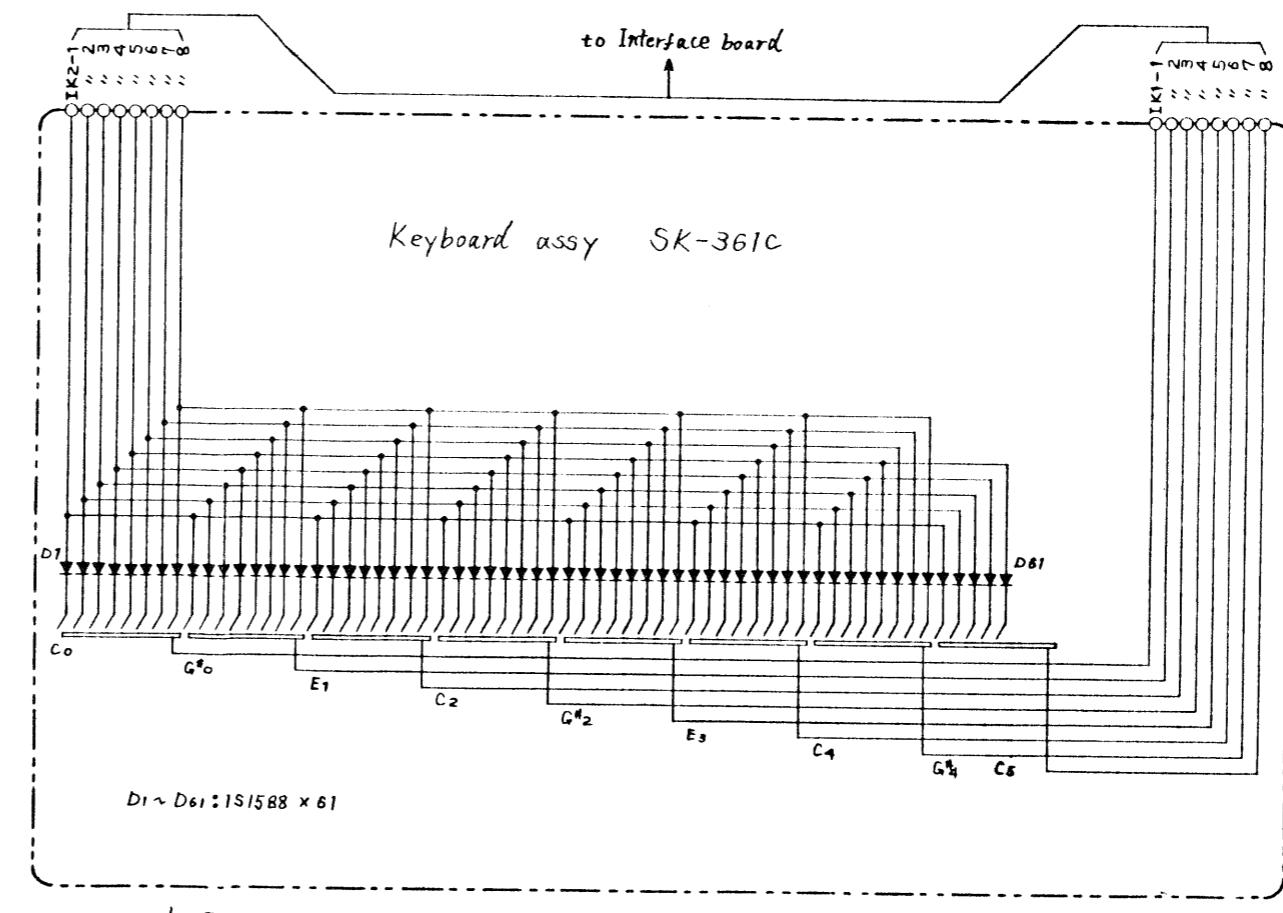


See pp. 34–35 for  
SN171700 and up

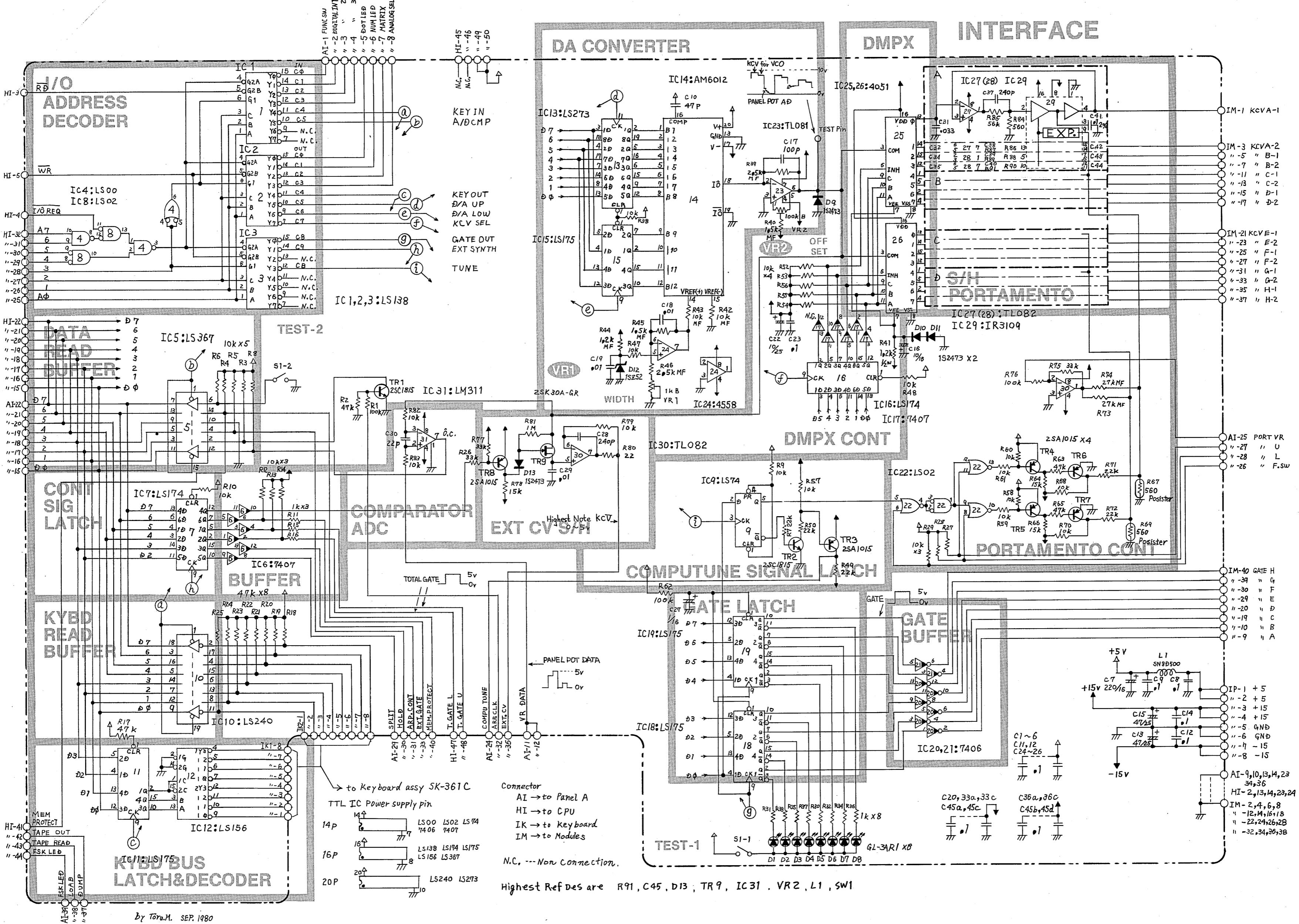
## CAUTION

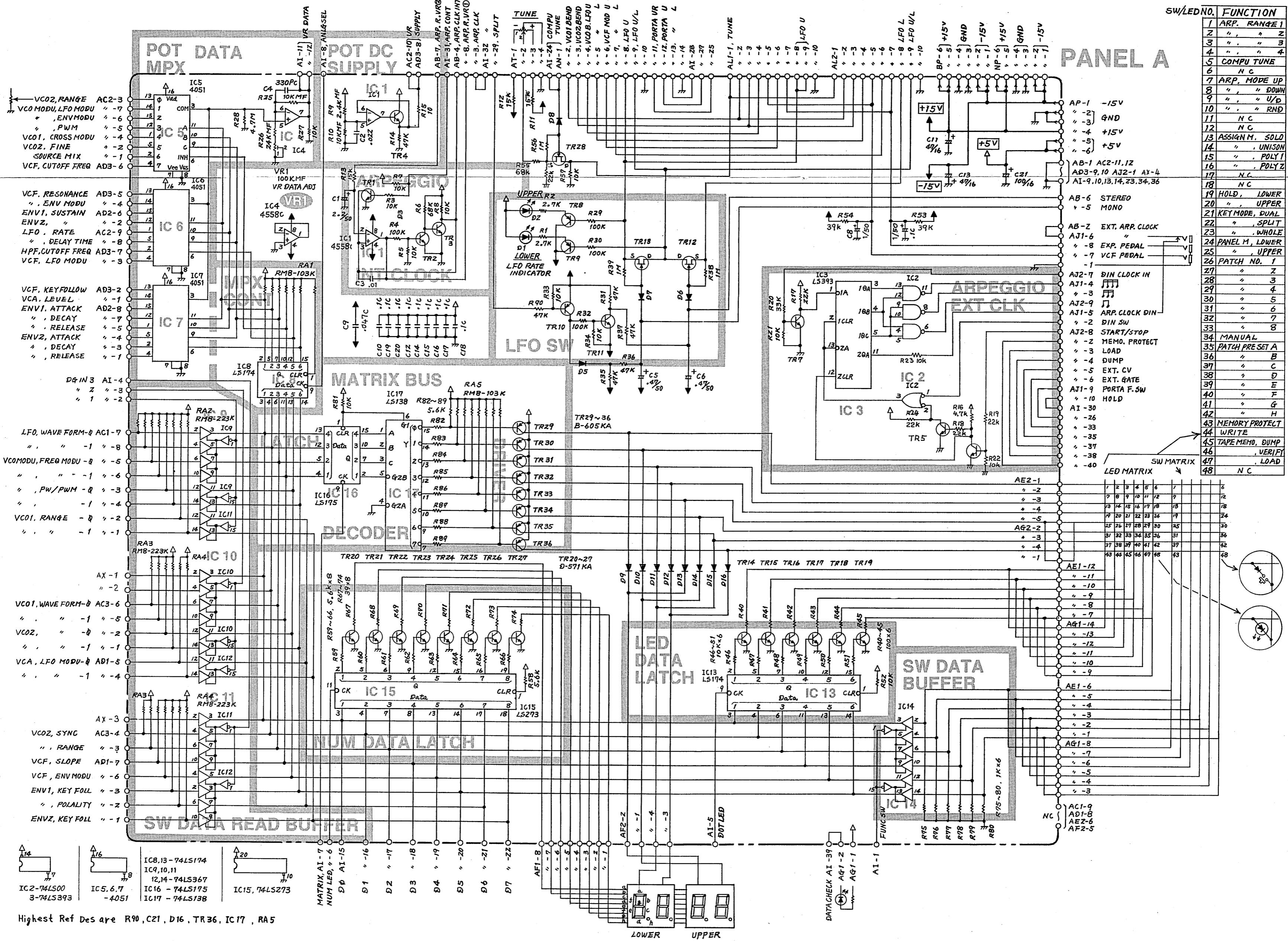
When replacing Interface board bearing edition no. 052H268 (and below) with PCB of 052H268 (and above), refer to pp. 34 and 35 for PROMs versions of CPU board.

	R25J		2SC1815-GR
	CRB25FX		2SA1015-GR
	POSISTER		2SK30A-GR
	ERS-C334561		
	R50J		
	ET-6P		1S2473
	TL082		15252
Selected on current leakage			LED GL-3ARI



A B C D E F G H I J K L M N O P Q R S T U V W X Y Z



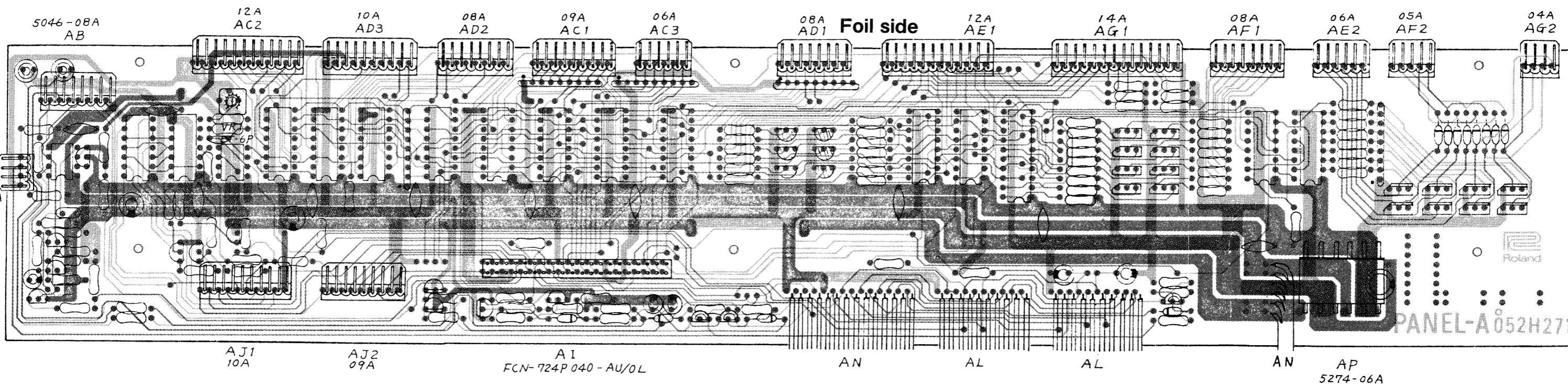
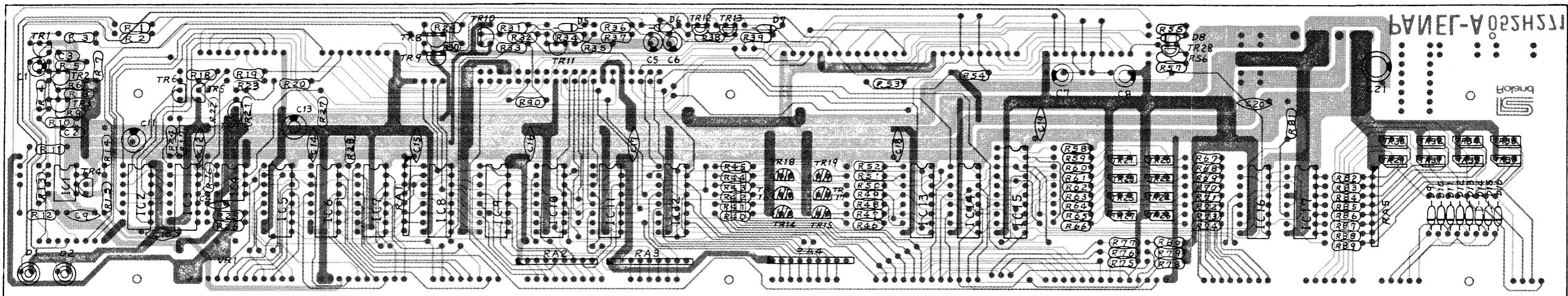


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42

## PANEL BOARD A OPH125(149H125) (pcb 052H271)

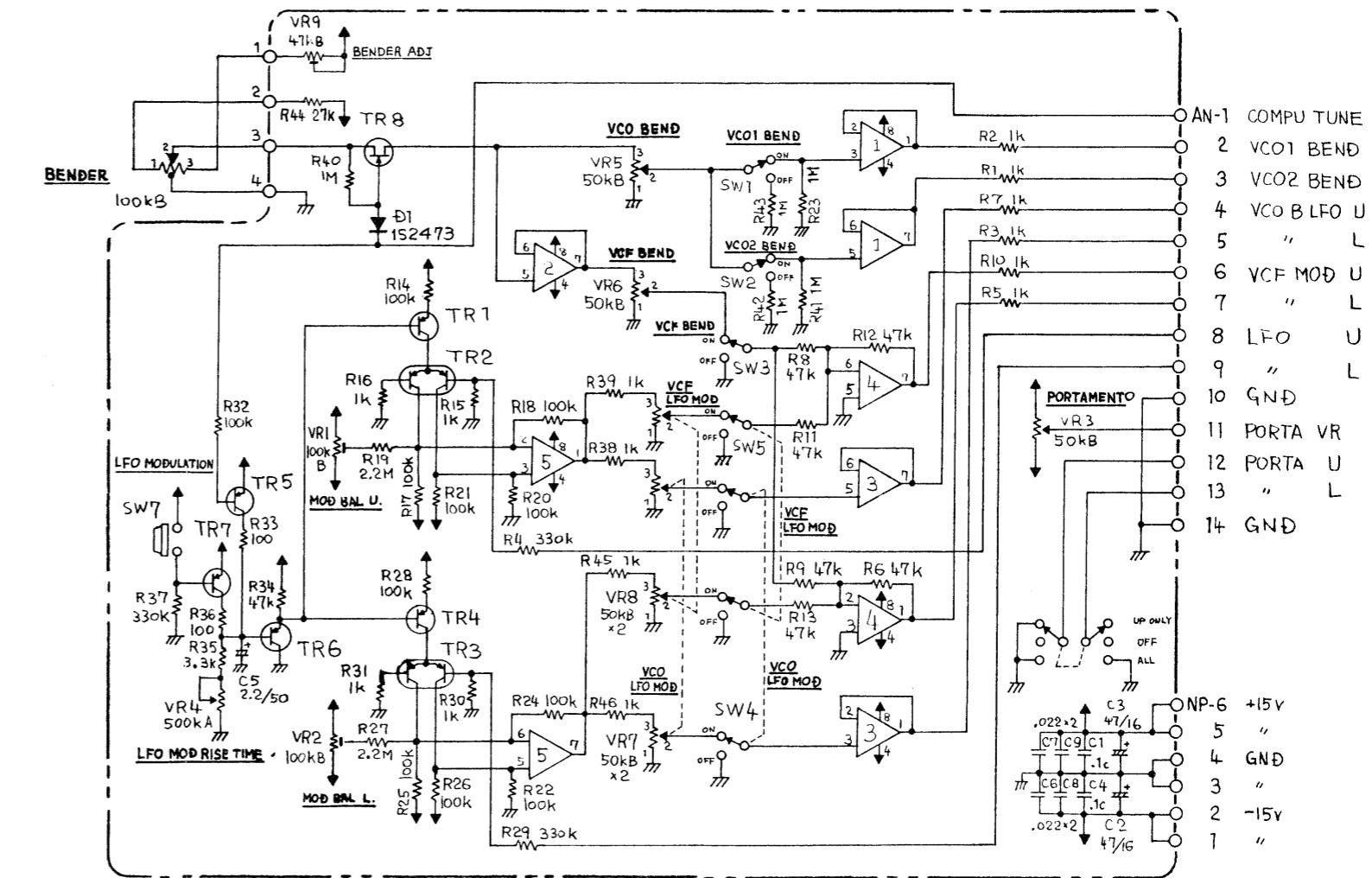
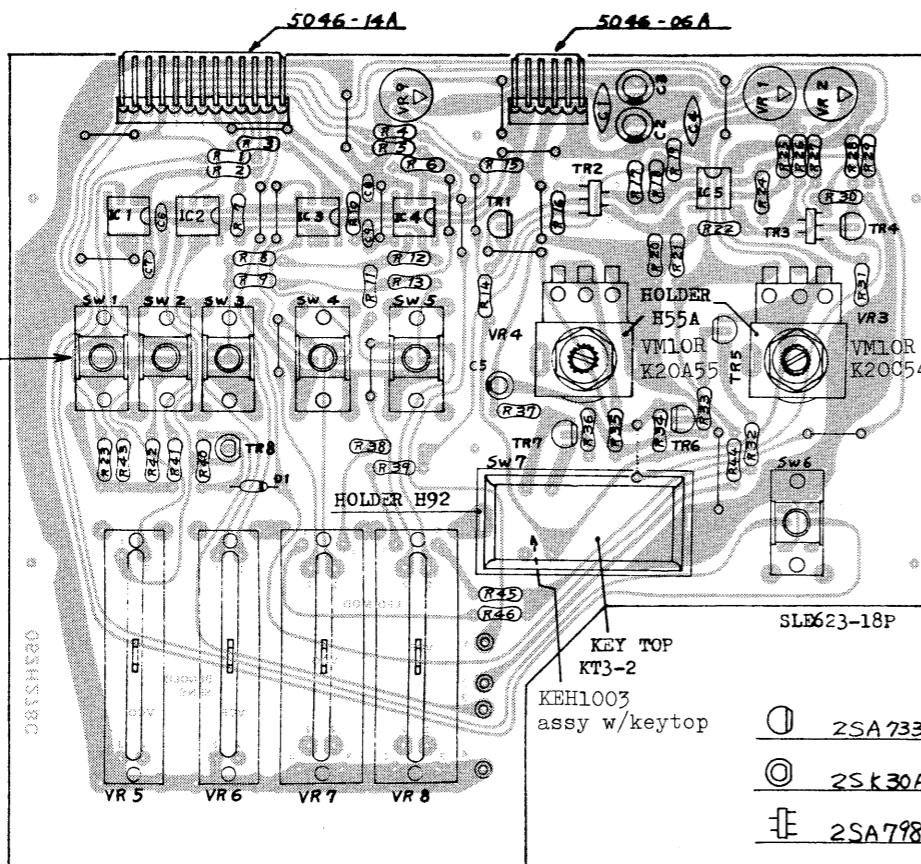
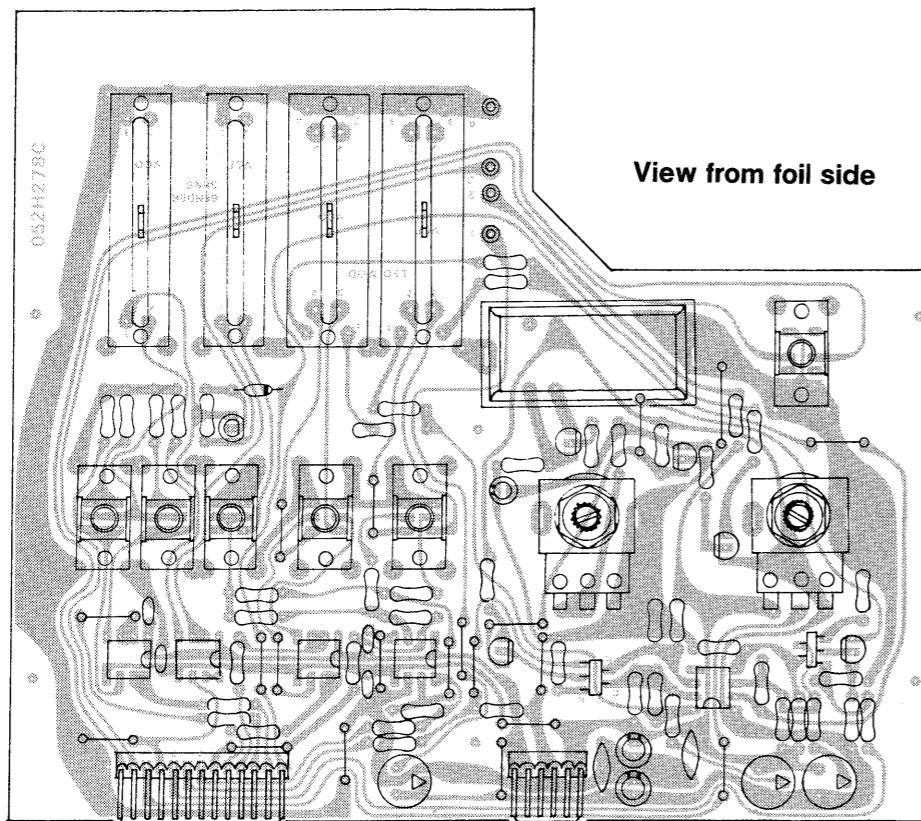
- A1015 Y or GR
- D571KA
- R25J
- C1815 Y or GR
- K30AGR
- CR825FX
- C1815 GR
- 152473
- B605 KA
- Resistor array

## Component side



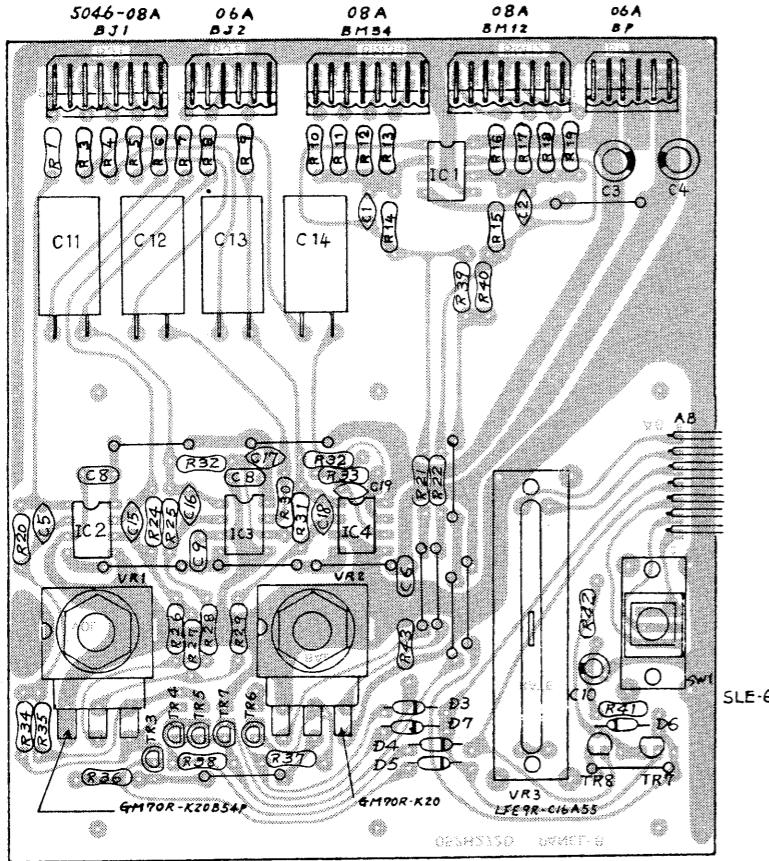
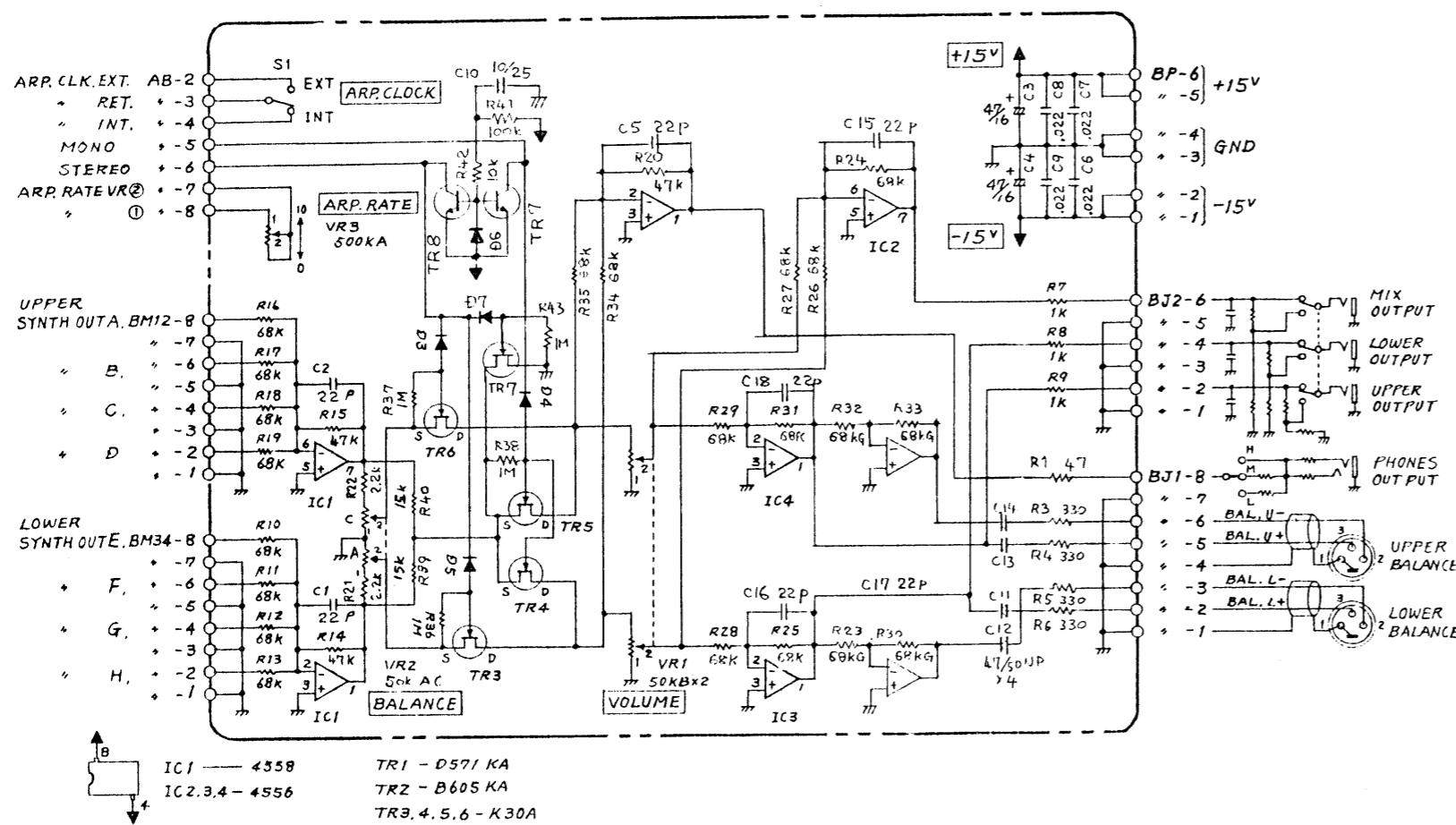
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

A  
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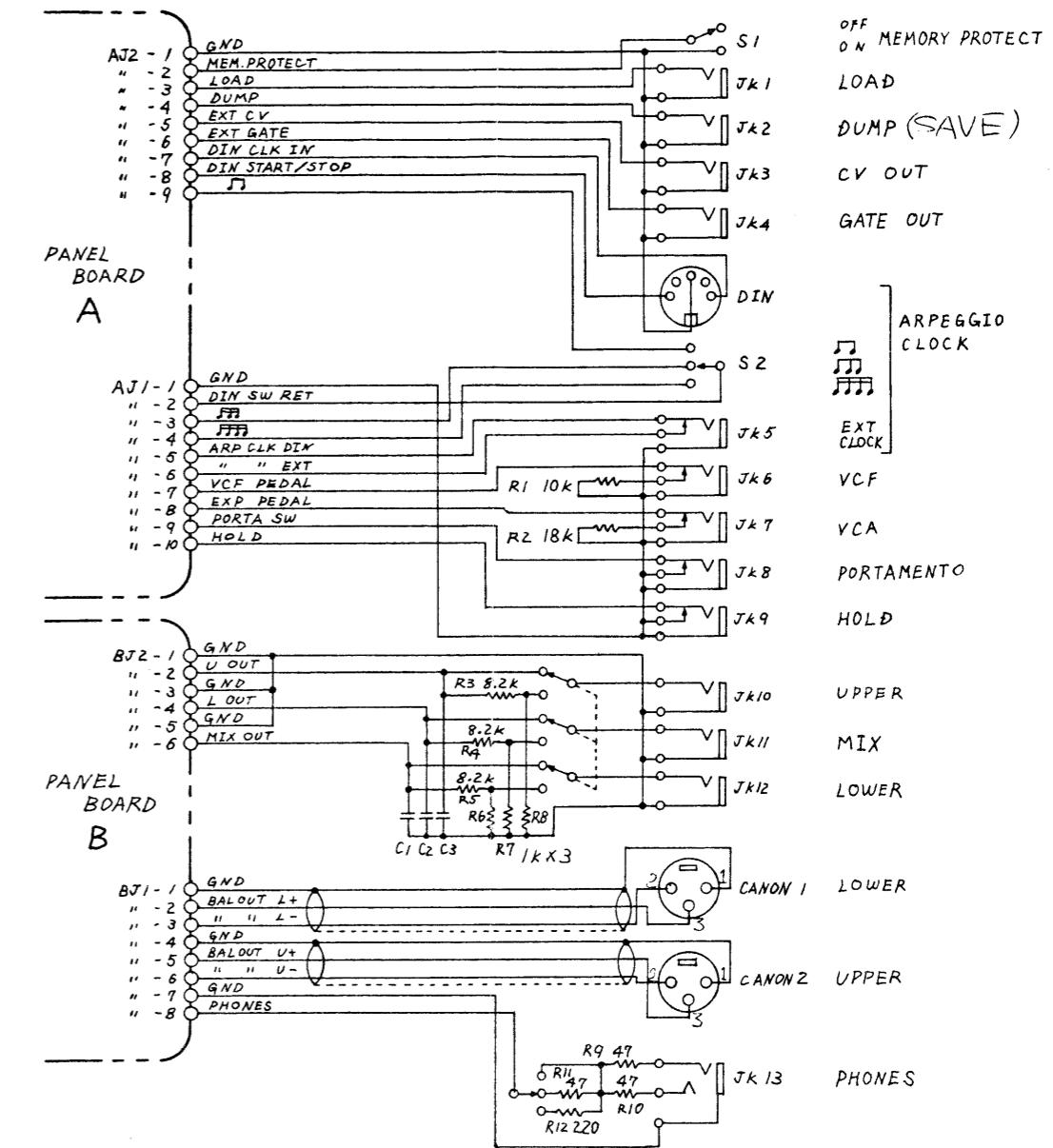
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

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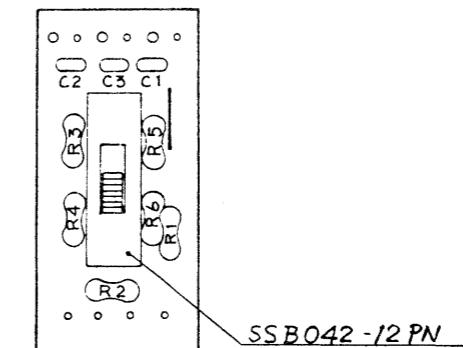


**PANEL BOARD B**  
**OPH126(149H126)**  
**(pcb 052H272)**

 R25J  
 1S2473  
 2SK30A  
 2SC1815 GR

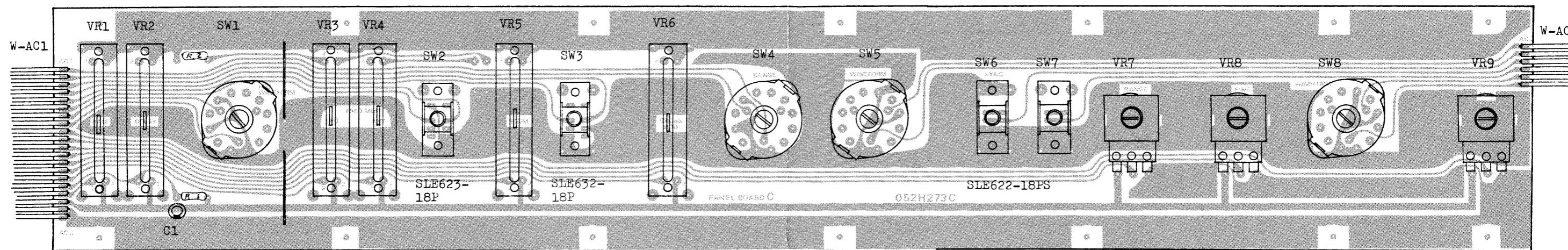


**LEVEL SELECT BOARD**  
**OPH139(149H139)**  
**(pcb 052H330)**

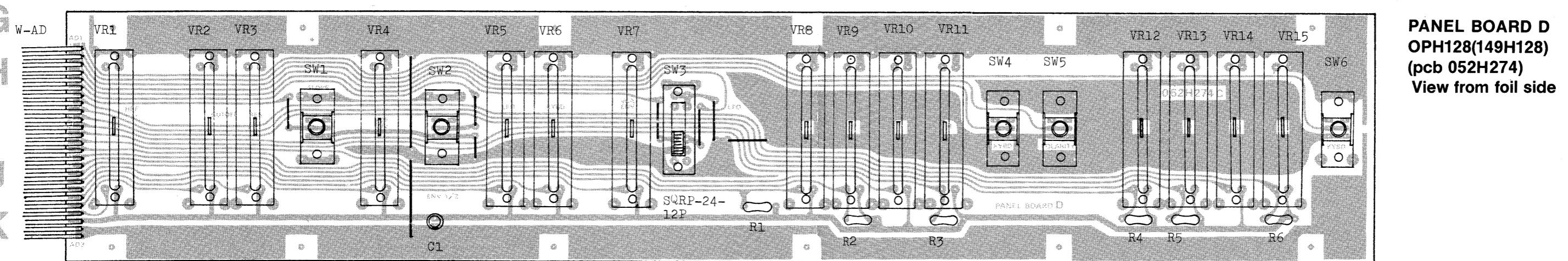


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

PANEL BOARD C OPH127(149H127)(pcb 052H273) View from foil side

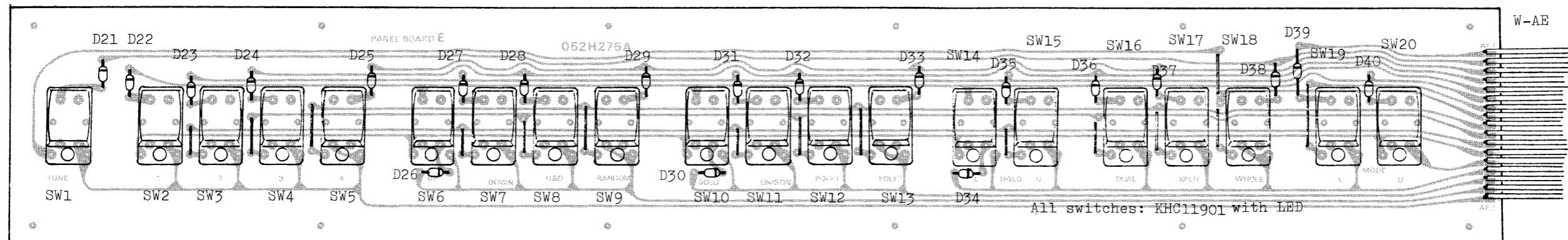


All sliders: LFE9RC16B14 All rotary pots: VM10RK20B14 All rotary switches: SRM1034-K15

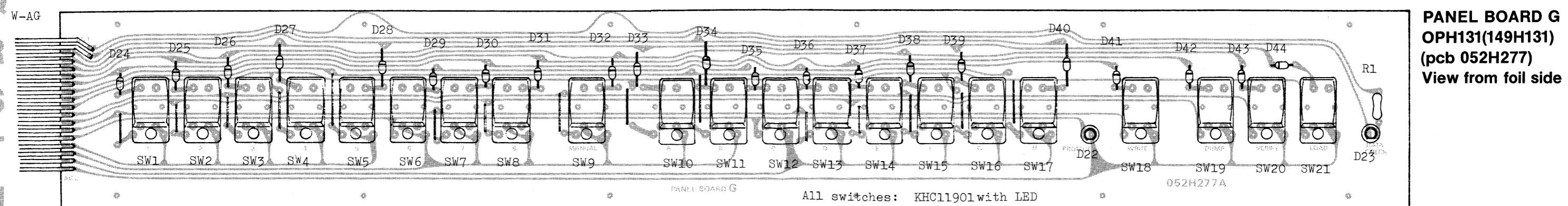


PANEL BOARD D  
OPH128(149H128)  
(pcb 052H274)  
View from foil side

All sliders: LFE9RC16B14 All lever switches: SLE622-18PS



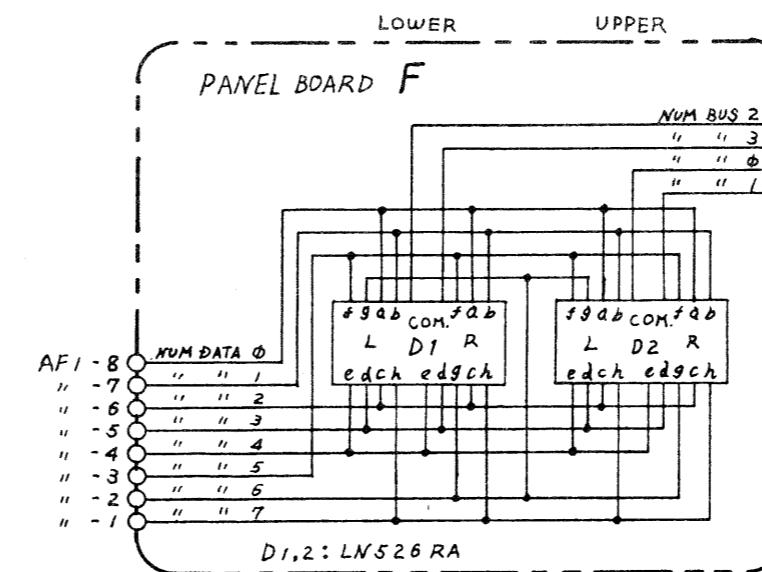
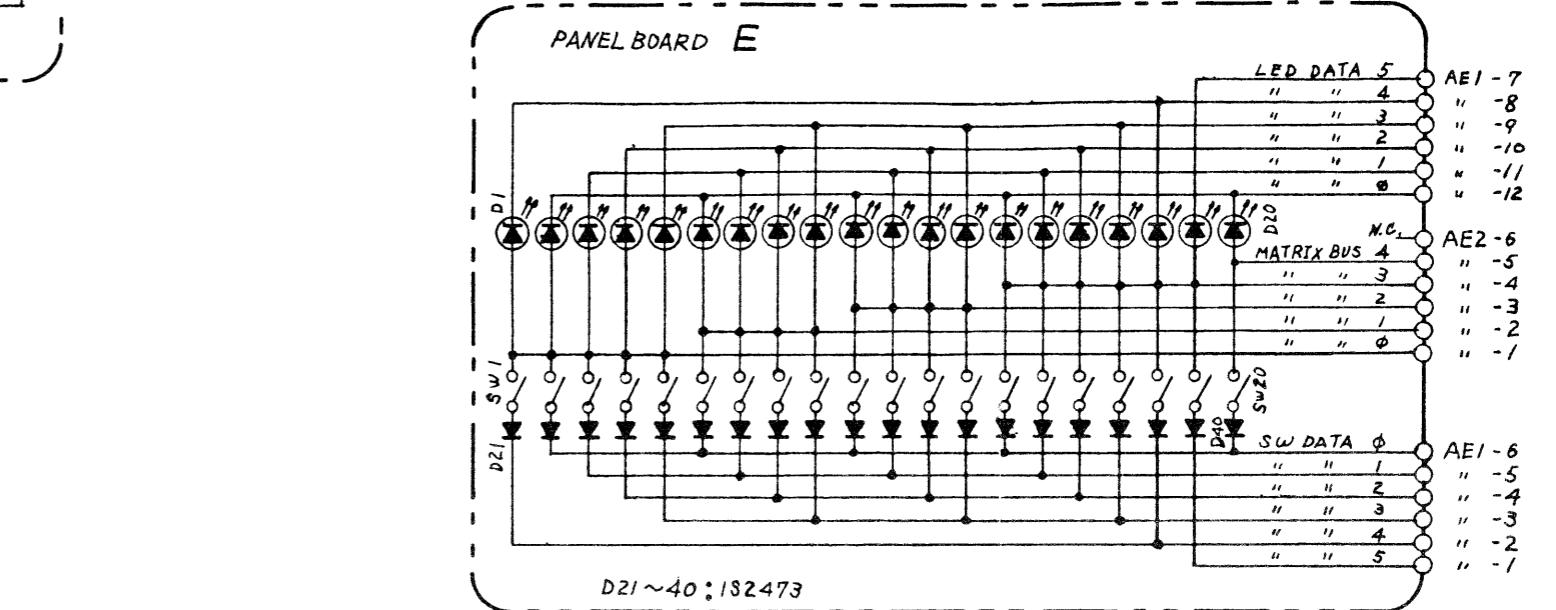
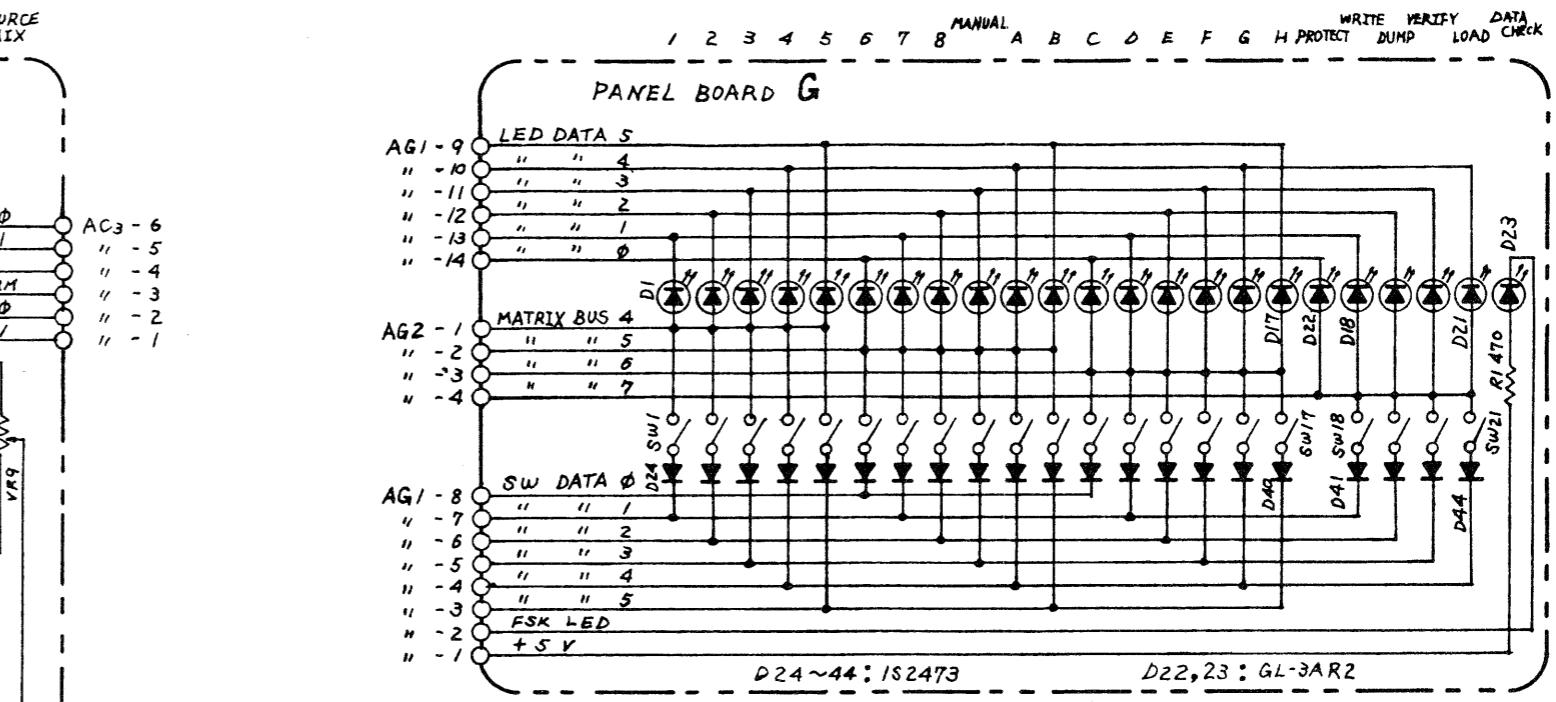
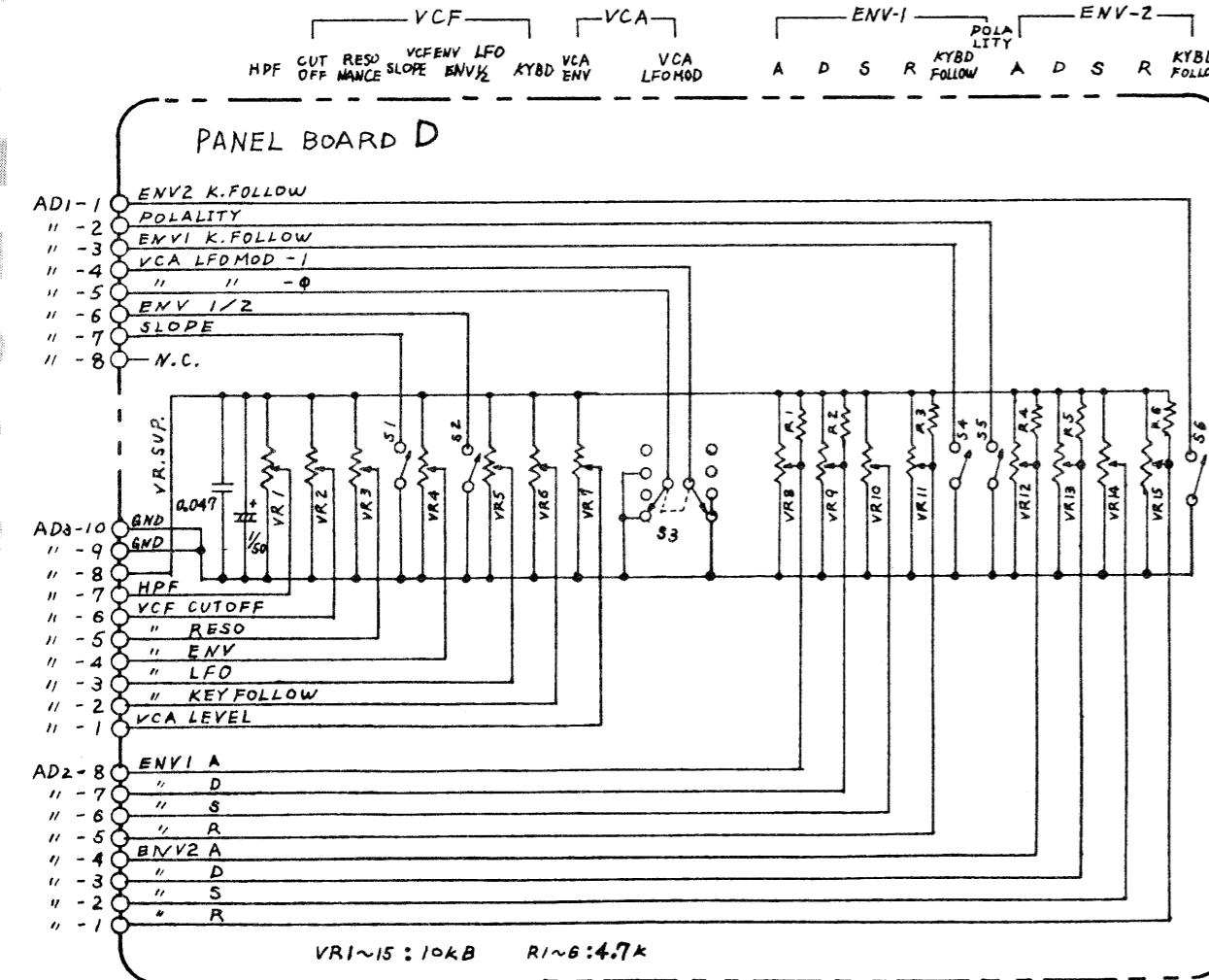
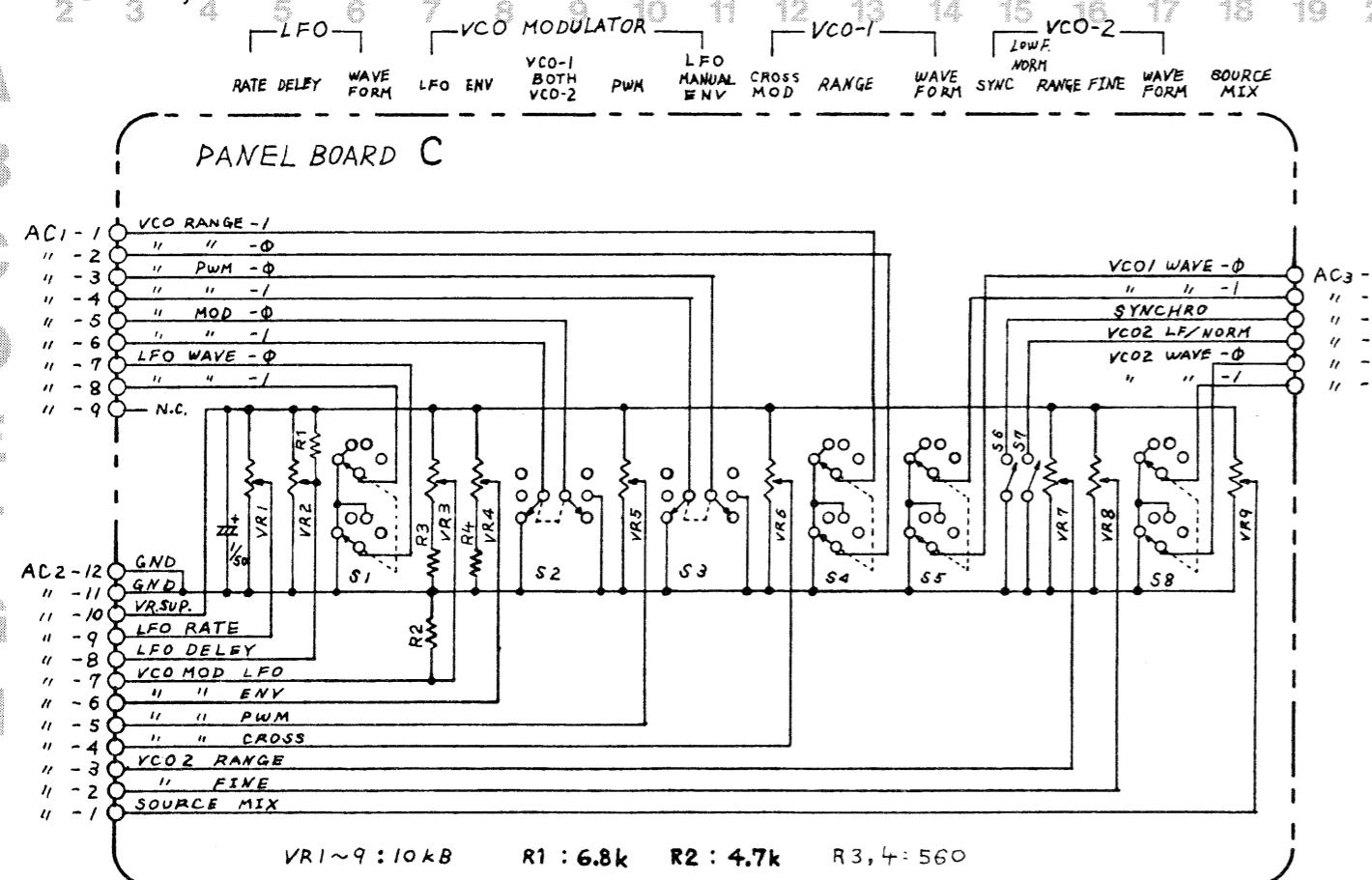
PANEL BOARD E  
OPH129(149H129)  
(pcb 052H275)  
View from foil side



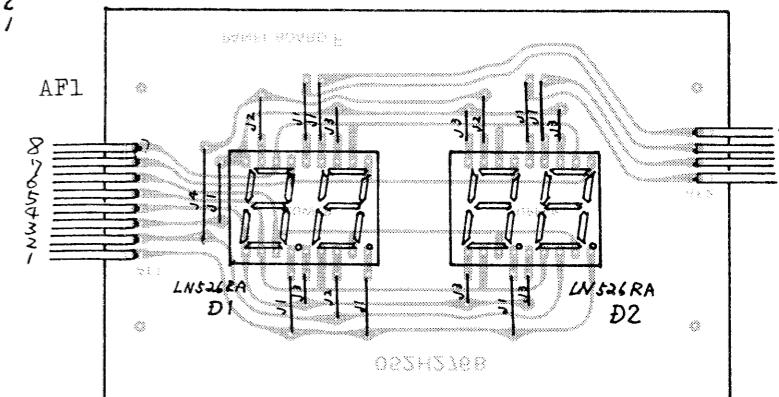
PANEL BOARD G  
OPH131(149H131)  
(pcb 052H277)  
View from foil side

OCT.10, 1981

JP-8

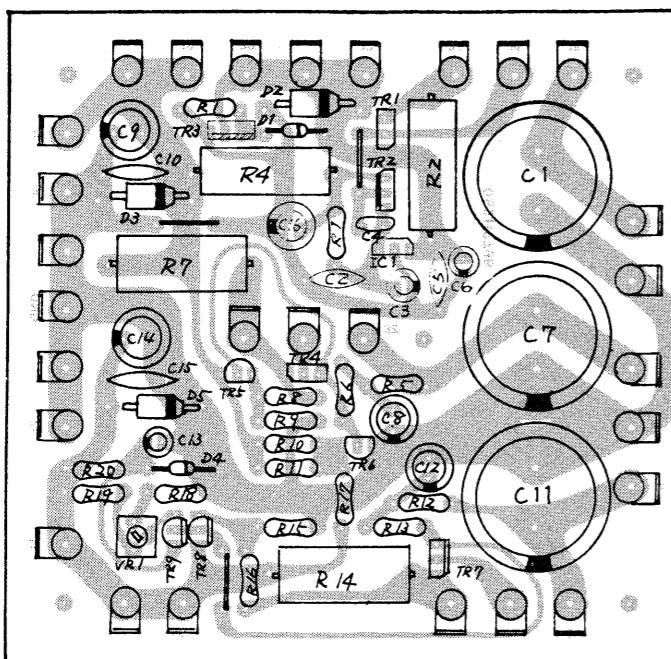


**PANEL BOARD F**  
OPH130 (149H130) (pcb 052H276B)



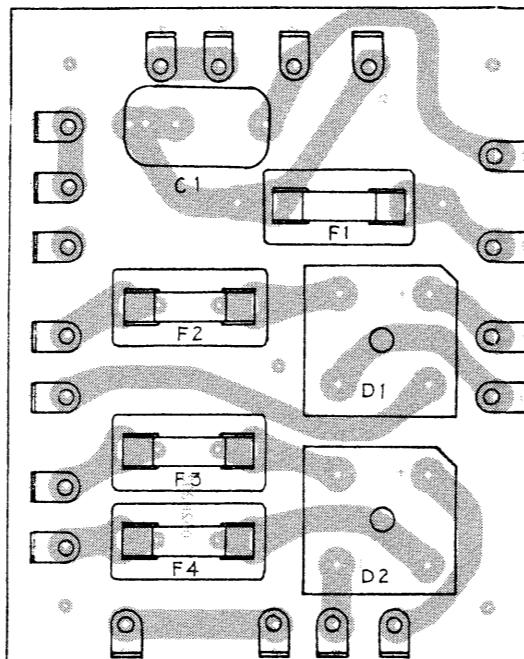
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

**POWER SUPPLY BOARD A**  
PSH059(146H059)(pcb 052H279)

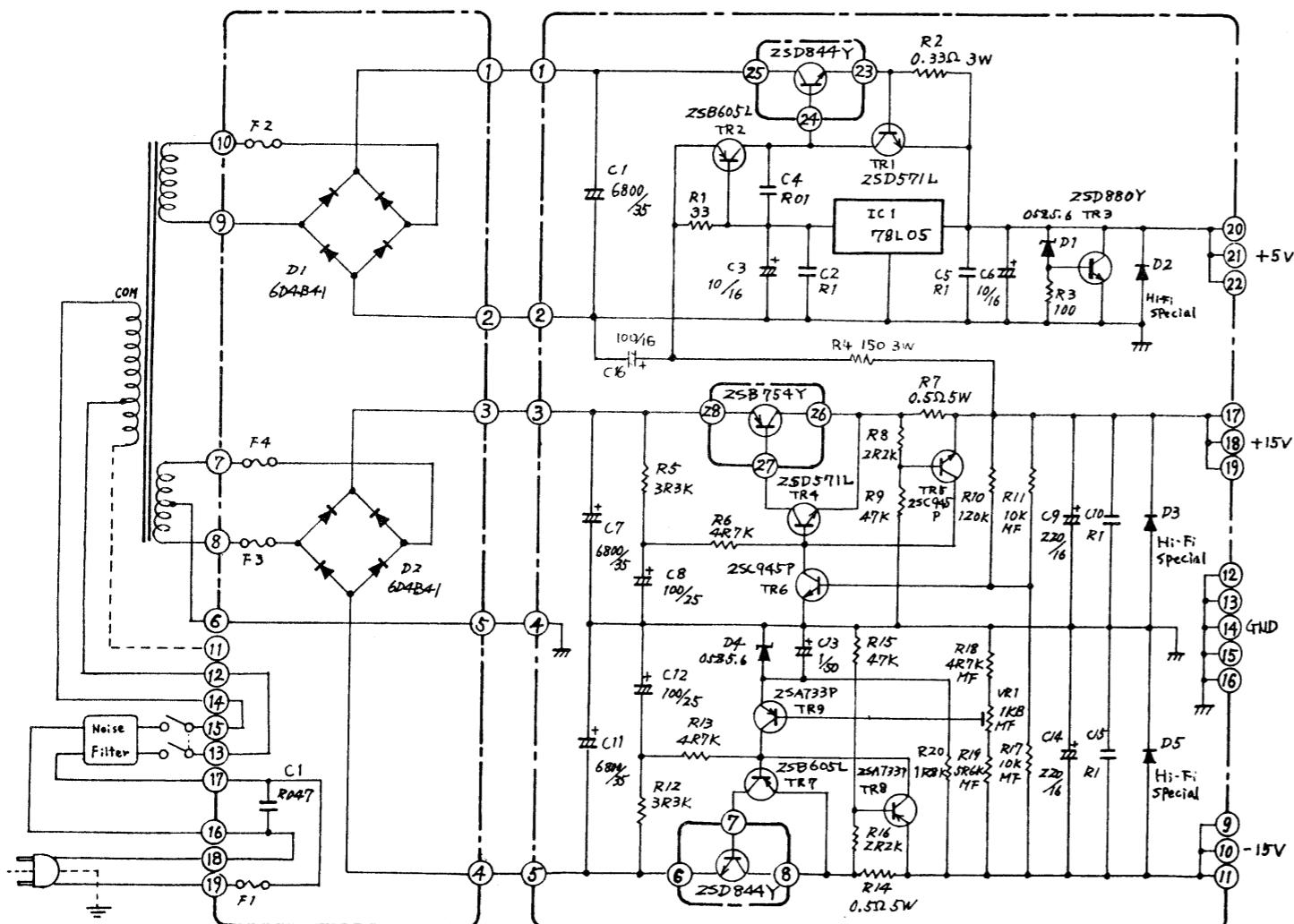


POWER TRANSFORMER SECONDARY RATINGS  
±20.5VDC @ 1.3A 4700μfd IN  
±8.5VDC @ 1.3A 4700μfd IN

**POWER SUPPLY BOARD B**  
PSH061(146H061) 100/117V  
PSH062(146H062) 220/240V



100/117V 220/240V  
F1 MGP0003 (3.0A) CEE Tl.6A  
F2 none CEE T5.0A  
F3 none CEE T5.0A  
F4



This is an 8 bit parallel CPU and is compatible with Z-80A and LH0080A.

- \* Instruction sets: 158
- \* Instruction cycle: 1.0μs (4.0MHz)
- \* Internal registers: 17
- \* Address bus: 16 bit
- \* Data bus: 8 bit

#### PIN FUNCTIONS

**ADDRESS BUS** Transfers 16 bits to memory address decoders (CPU board- IC21, 22 and 23) for controlling the followings:  
on CPU board - ROM, CMOS, RAM, N-ch RAM, TAPE and TUNE reading.  
on MOD CON board - RAM, UP, LO and VCO select.  
Lower 8 bits are transferred to I/O Address decoders (Interface board - IC1, 2, 3, 4 and 8) for controlling the followings:  
IN - Function sws, Digital IN (1, 2 and 3), Key IN, A/D.  
OUT - Dot LED, Num LED, Matrix, Analog sel, Key out, D/A Up/Lo, KCV sel, Gate out, EXT synth, Tune.

**DATA BUS** Used to transfer 8 bit instructions and data between CPU and memories or I/O device.

**Ø** Square wave, 4 MHz. Derived from X-tal oscillator's 8 MHz, divided-by-two through frequency divider.

**MRQ (Memory Request)** Indicates that Address bus holds a valid memory address for a memory read and memory write.

**IORQ (I/O Request)** Indicates the presence of I/O Device number at pins A0-A7 during I/O write/read cycle.

**RD (Memory read)** Indicates that CPU wants to read data from memory or I/O device. The addressed memory or I/O device outputs data onto the CPU data bus at positive transition of RD.

**WR (Memory write)** Indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device which latches the data off of the bus at positive transition of WR.

**INT (Interrupt Request)** Whenever INT (Ø, frequency divided by Counter-2, IC40) is fed to CPU every 1ms via IC26, it accepts INT upon finishing processing job then starts executing Panel LED lighting program, generating INT Acknowledge as an IORQ in M1 cycle.

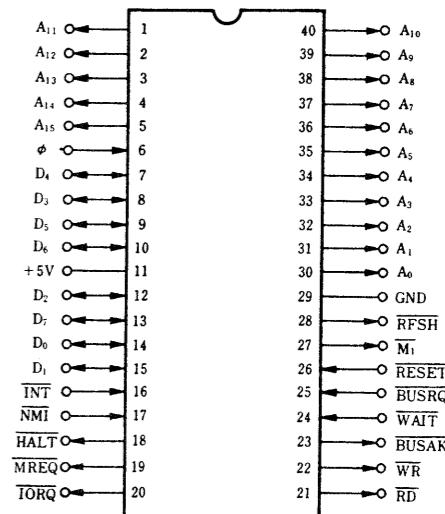
**WAIT** Lengthens read or write cycle until data on the data bus becomes valid during the presence of address signal for timing CPU access time to memory or I/O device.

**RESET** Initializes CPU circuits upon power on for the JP-8 or when DC voltages drop below specified value.

**μPD780 C/D-1**

#### 8 BIT MICROPROCESSOR

##### (Top View)



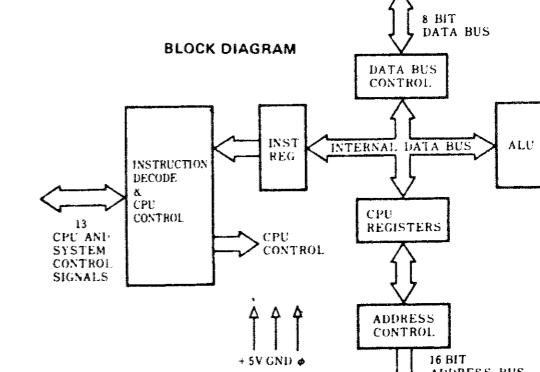
#### REGISTERS

MAIN REG SET		ALTERNATE REG SET	
ACCUMULATOR A	FLAGS F	ACCUMULATOR A	FLAGS F
B	C	B	C
D	E	D	E
H	L	H	L

GENERAL PURPOSE REGISTERS

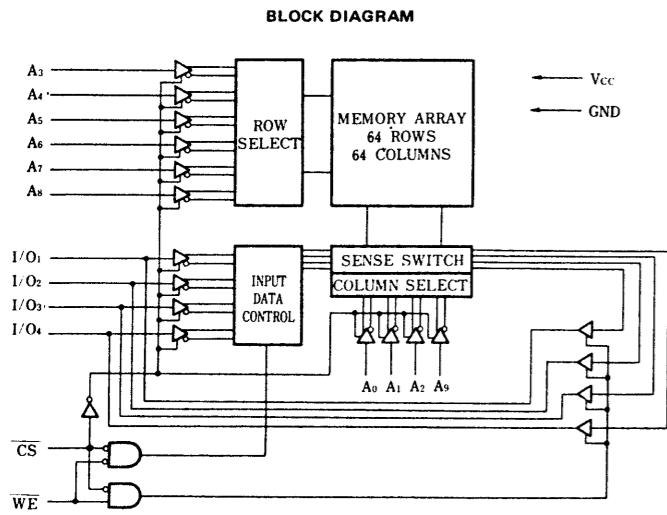
INTERRUPT VECTOR	MEMORY REFRESH R
INDEX REGISTER IX	
INDEX REGISTER IY	
STACK POINTER SP	
PROGRAM COUNTER PC	

SPECIAL PURPOSE REGISTERS

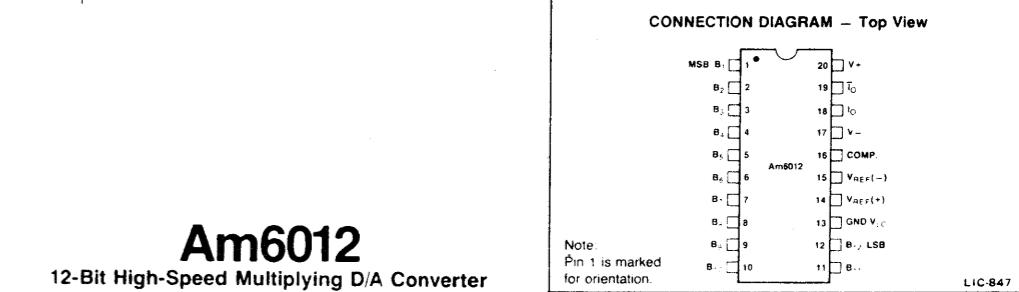
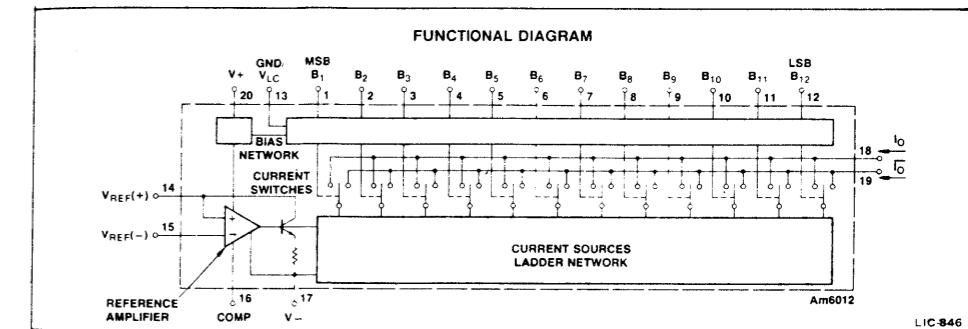
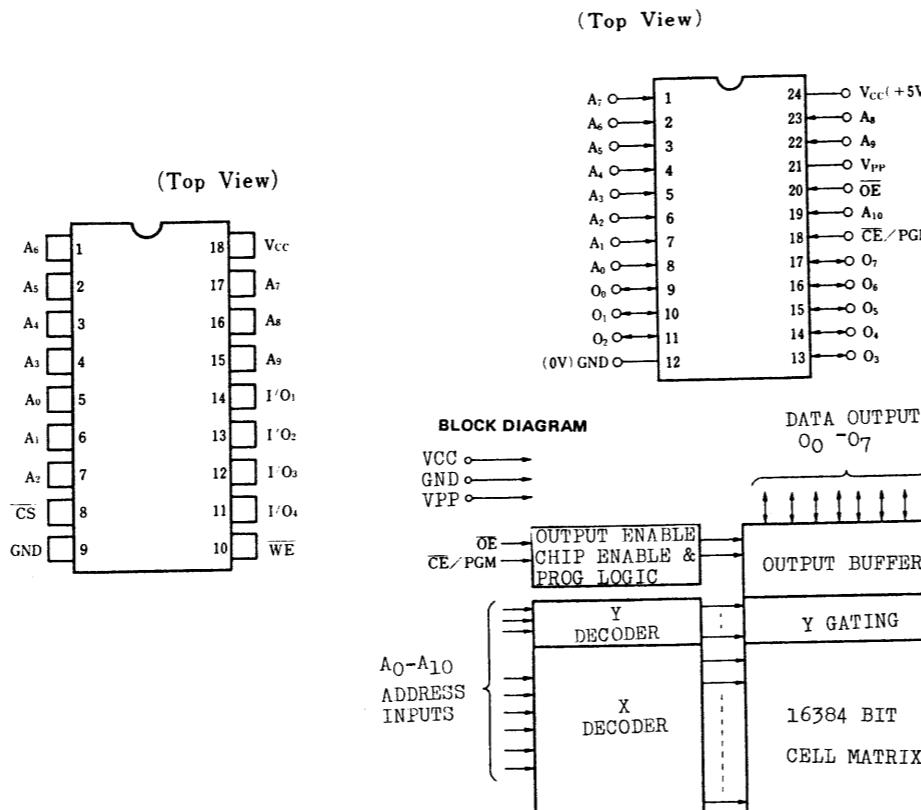


OCT.10, 1981

**$\mu$ PD444C**  
1024 X 4 BIT STATIC RAM CMOS RAM

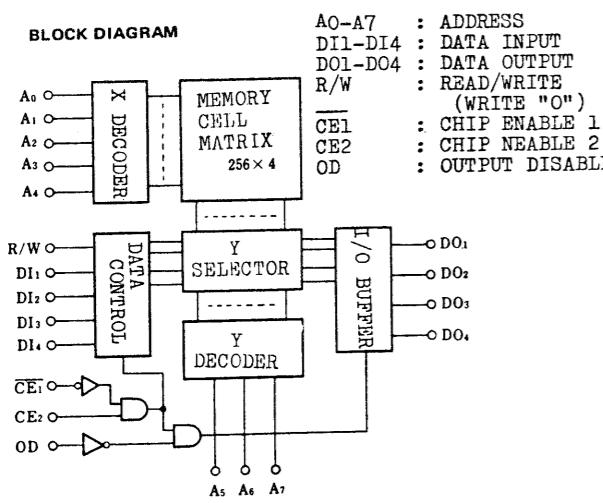
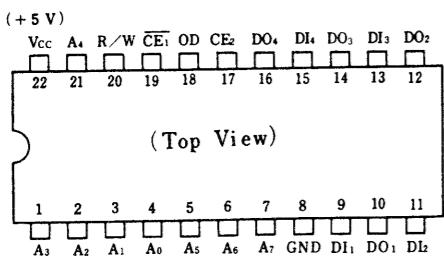


**$\mu$ PD2716D**  
16K (2K x 8) UV ERASABLE PROM



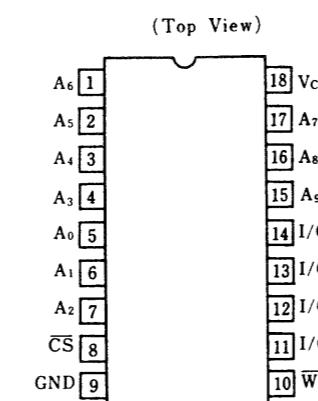
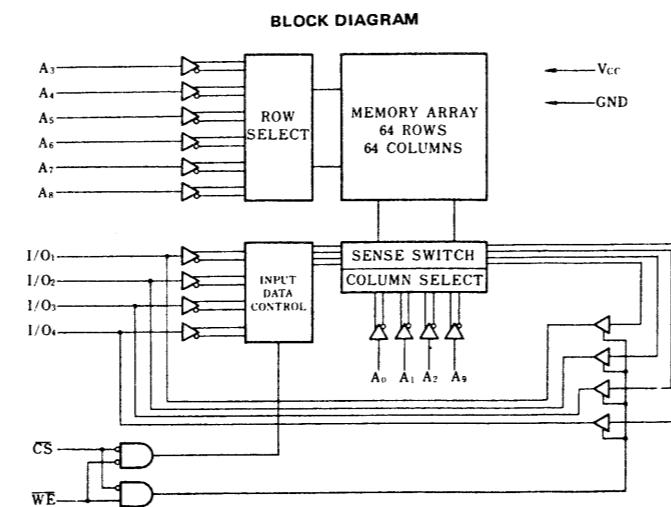
**$\mu$ PD2101ALC**

1024 BIT (256x4) STATIC MOS RAM



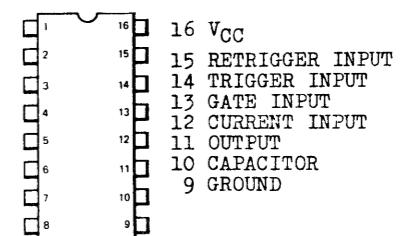
**$\mu$ PD2114LC/D**

1024 X 4 BIT STATIC RAM

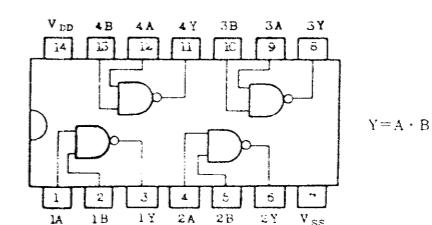


**IR3R01**

- 1 MODE INPUT
- 2 ATTACK TIME INPUT
- 3 DECAY TIME INPUT
- 4 RELEASE TIME INPUT
- 5 SUSTAIN VOLTAGE INPUT
- 6 COMMON INPUT 0.3V
- 7 REFERENCE VOLTAGE
- 8 V<sub>EE</sub>



TC40H000P QUAD 2-INPUT NAND GATE



## ADJUSTMENTS

### DISASSEMBLY

Follow procedure on page 2. Preparation of a STAY (chain or string) and prop is advisable for a stable top panel rest.

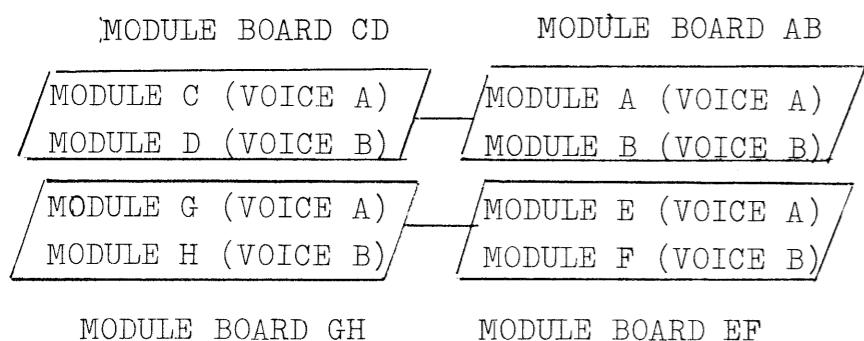
### PRECAUTIONS

Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, most circuits are temperature-sensitive.

The adjustments on the JP-8 should not be done more than necessary. Adjustments merely attempted on a particular module (VOICE) might cause sound balance away from entire VOICES and can, in an extreme case, require the same procedures to be done fifteen times for the remainder.

### DESIGNATION – TEST POINT, TRIMMER, PCB –

For PCBs that are identical in circuit configuration, most adjustment steps, test points and trimmers do not refer to a particular PCB or module (VOICE), they may be read as ones on a PCB to be adjusted.



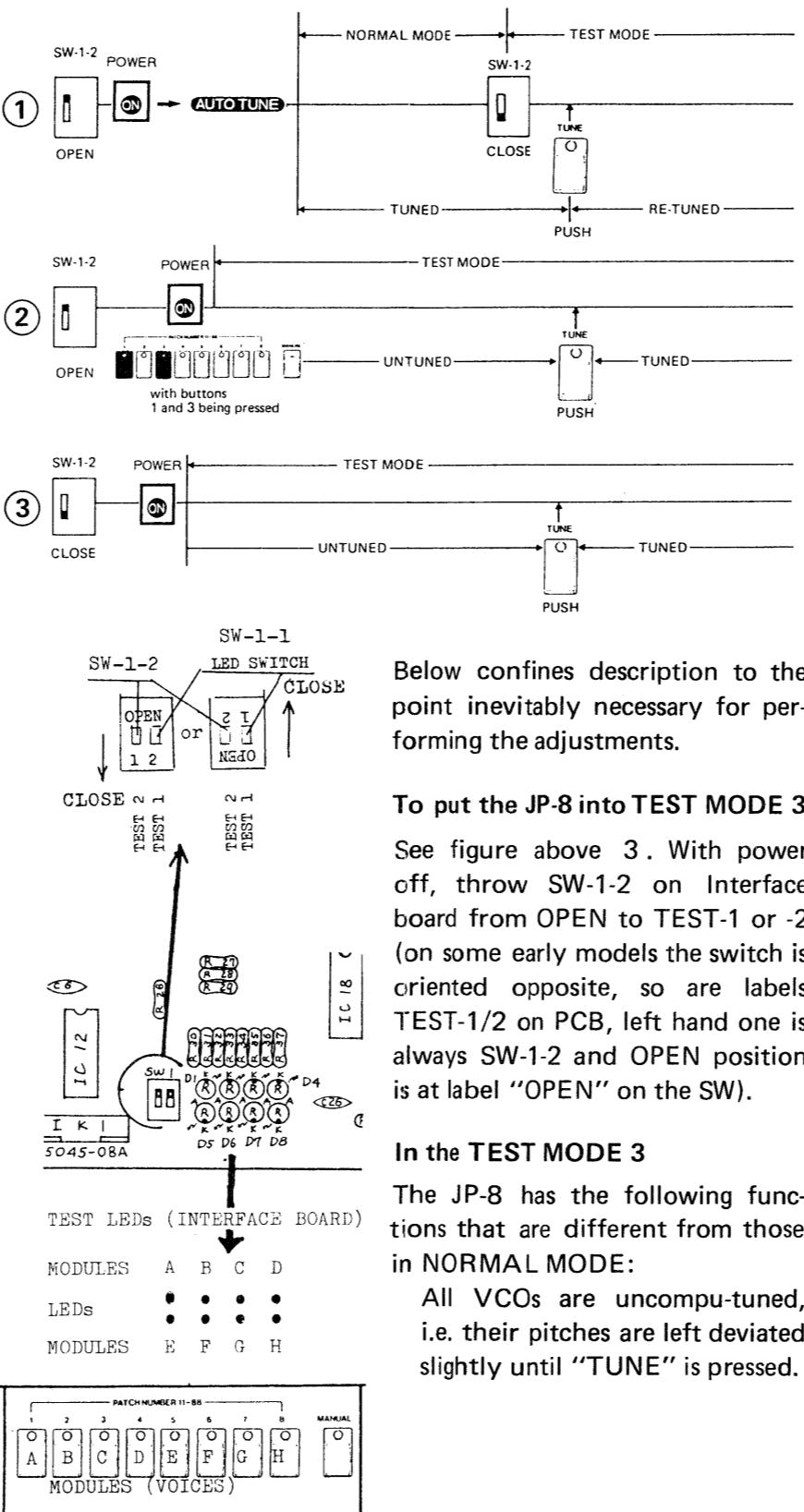
Four module boards, each consisting of two voices, are identical in all aspects, having the same designators with A or B suffix for the same components of two VOICES, e.g. VR1A (VOICE A) and VR1B (VOICE B). Note that each voice contains two VCOs, VCO-1 and VCO-2.

### ADJUSTING ORDER

The adjustments proceed from paragraph 1, DC Supply assuming that the JP-8 is completely unadjusted. When adjusting a specific section, begin with lower numbered para. in the relative adjustment section, e.g. first No. 7 BAL, then, No. 8 DEPTH, as directed.

### TEST MODES

Adjustments on the JP-8 proceed in TEST MODEs. Although three TEST MODEs are available for the adjustments, TEST MODE (3) is chosen in this manual unless otherwise specified. (For more details refer to TEST MODE in Circuit Description – separate copy.)



- \* Among key assignments, POLY-1 only changes assigning order – tapping single key (same key) will assign modules from A to H one by one, repeating the order. This is convenient in comparing 8 modules sounds (timbre, pitch, etc.) sequentially at a note.
- \* Computer provides FSK adjustment (para. 26) program and outputs test signal at SAVE (DUMP) jack when VERIFY is pressed.
- \* Integrated PATCH NUMBER LEDs serve as module (VCO) indicator for visible checking, identifying VCO(s) being directed by key(s) has been depressed or being held down.

SW-1-1, LED switch, in close position, allows LEDs (TEST LED) located right to it to be energized regardless of MODE (NORMAL or TEST) when gate signals are fed to them individually. The LEDs function as assignment indicator just as Patch Number LEDs do. Test LEDs find extended application for learning and checking the assignments varying to MODEs (KEY, PANEL and ASSIGN) in Normal mode.

Patch Number LEDs are lit automatically in sequence immediately after TUNE is touched, representing module A VCO-1 (leftmost LED), A VCO-2 (No.2 LED) and so on; the first cycle for Upper modules' and the second for Lower. Their lighting period is proportional to degree of VCO detune from standard pitches. An LED staying on and won't pass illumination to the next one claims checking of its mated VCO having been far out of computer controllable range.

TEST MODEs 2 and 3 are identical to each other in function, but any panel disassembly is required for mode 2 if the purpose is only to check Key Assignment or VCO detune.

### FOR SATISFACTORY SERVICE WORK

1. Dump user's preset memory on tape before attempting adjustments and troubleshooting.
2. If TUNE was pressed in previous adjustments, be sure to power off and on the JP-8 before making adjustment which must be done without compu-tune.
3. Plural keying and miskeying will disorder key assignment sequence. Push HOLD or ASSIGN MODE to off and again to on, as appropriate, to restore the order. Use monitor amp to detect erroneous key assignmanet that LED does not distinguish.
4. Make a practice of pushing MANUAL after changing PANEL MODEs.
5. Restore SW-1-1 and SW-1-2 to OPEN and load back the data on tape before return the unit to the customer.

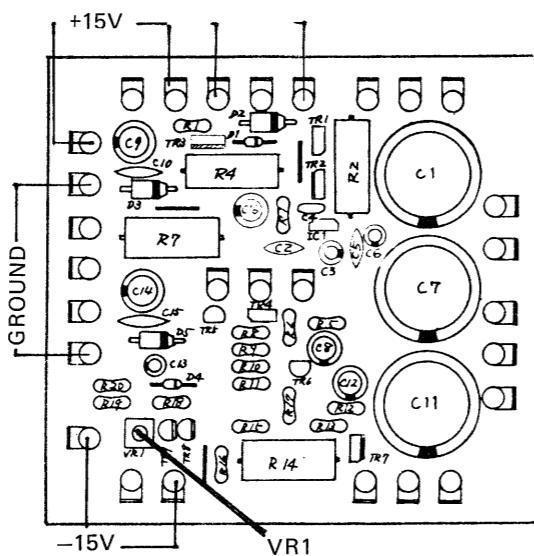
## BEFORE STARTING ADJUSTMENTS

ALLOW AT LEAST 30 MINUTES FOR WARUP PERIOD

## 1. DC SUPPLY

## POWER SUPPLY BOARD

1. Connect Digital voltmeter (DVM) to  $-15V$  (terminal 9, 10, 11).
2. Adjust VR1 for  $-15V \pm 10mV$  reading.
3.  $+15V$  should be  $+15V \pm 500mV$ .
4.  $+5V$  should be  $5V \pm 400mV$ .



## 2. DC SUPPLY (VCO)

## MODULE. MODULE CONTROLLER

See appendices for adjustment locations and glossary.

## MODs A, B, C and D

1. Connect DVM to MOD AB IC1 pin 4 ( $-VDD$ ).
2. Adjust upper CON VR4 for  $-13V \pm 5mV$ .
3. IC1 pin 8 should read  $+13V \pm 200mV$ .

## MODs E, F, G and H

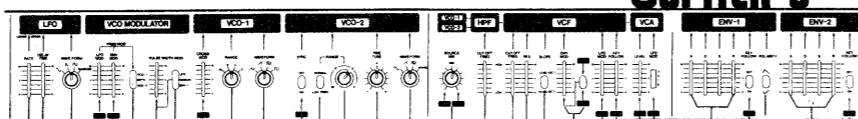
1. Disconnect flatcables at upper CON LM1 and HL. Observe the note in CON Layout, appendix.
2. Perform step 1-3 above for lower PCBs.

## 3. PANEL POTs VOLTAGES

## INTERFACE (INT) PANEL BOARD A

See appendices for locations and glossary.

1. Connect DVM to INT TP-3 or R83 (10k) lead facing outside. (See Fig. below right.)
2. Depress MANUAL.
3. Turn all the pots on the panel illustrated fully cw, or to 10. Incomplete settings result in a fluctuating reading or dips on a screen if observed with scope.
4. Set VR1 (Panel board A) for  $+5V \pm 2mV$ .

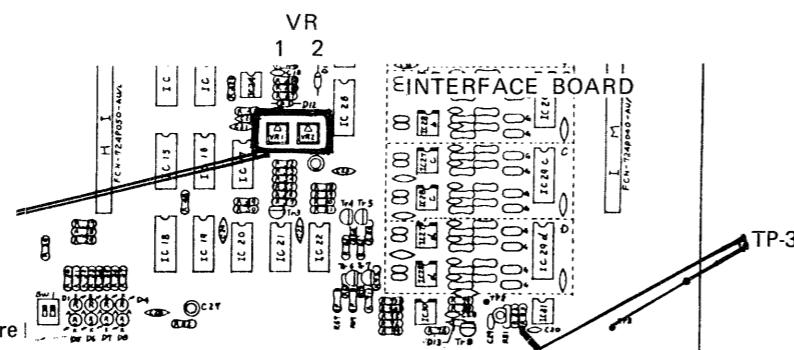


## 4. DAC

## INTERFACE (INT)

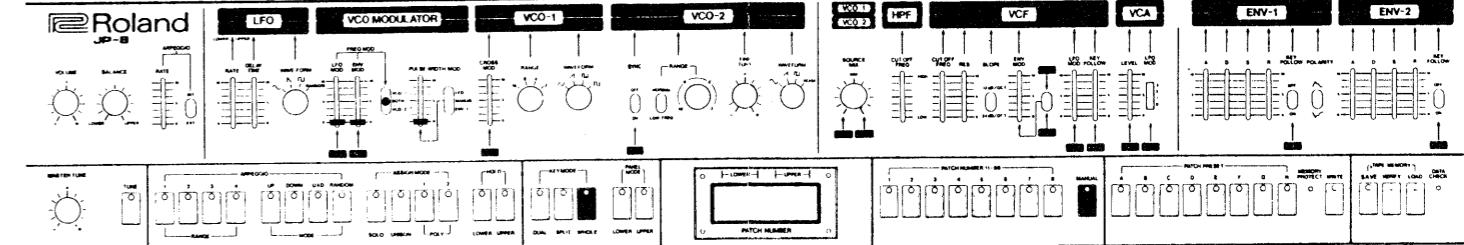
See appendix for glossary.

1. Connect DVM to OUTPUT CV jack.
2. Press KEY MODE WHOLE.
3. Press C0 key, adjust VR2 for 0.000V reading.
4. Press C5 key, adjust VR1 for 5.000V reading.
5. Check C0-C5 keys for scaling, that those voltages are  $1V/oct$  increments  $\pm 2mV$ .



## 5. VCO MOD BAL

## MODULE (MOD)

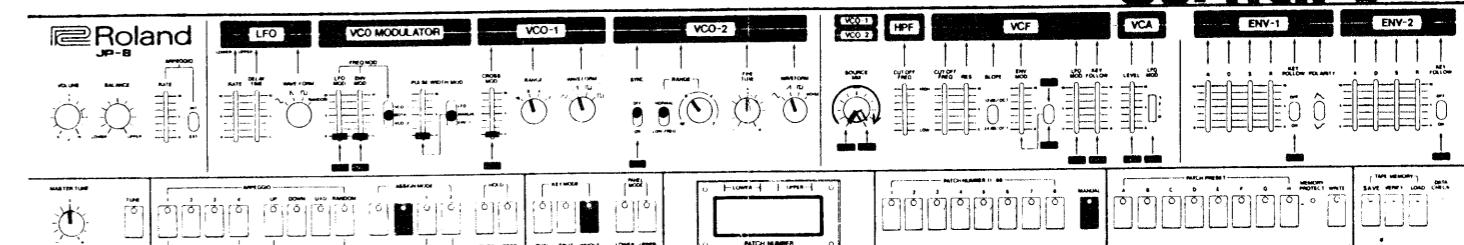


See appendices for adjustment locations and glossary.

1. Connect DVM to MOD TP-3 or R107 lead.
2. Adjust MOD VR7 for 0.000V reading.

## 6. VCO TUNE

## MODULE (MOD)



See appendices for adjustment locations and glossary.

Compu-tuned VCO needs to be re-calibrated only if it or associated components have been replaced. If a VCO is excessively out of tune right after compu-tune, first check MOD BAL, para. 5 and KCV OUT (INT terminals IM-1, IM-3, etc.) for voltage. Seconds, isolate possible causes before attempting VCO adjustments.

As is usual with tuning, several instruments may be used for determining frequency. The calibration proceeds by Lissajous figures with A-442 reference fed to scope's horizontal input.

1. Connect scope to MOD TP-4 or R130 lead.
2. Turn SOURCE MIX fully to VCO-1 or 2 accordingly.

## NOTE:

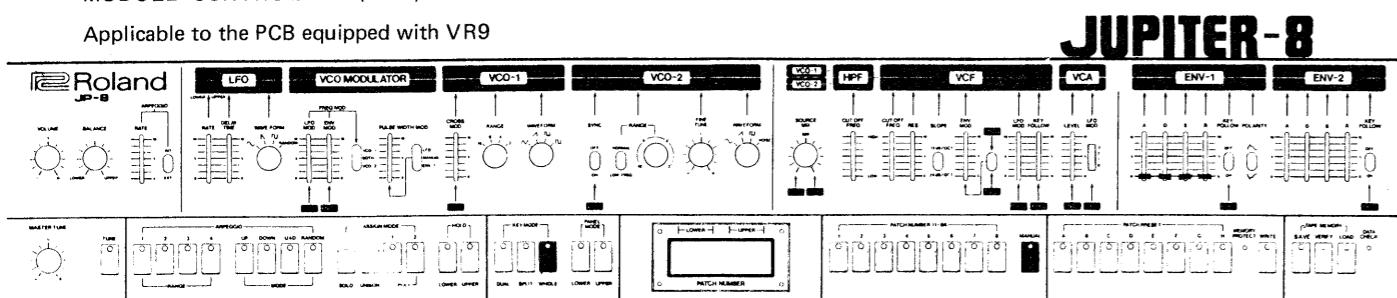
Make sure that the JP-8 is in the test mode without initially compu-tuned upon power on. To ensure this, turn power off and on. Then, push UNISON, etc. See "TEST MODE" on the first page of this section.

3. Press A3 key, adjust trimpot T for 884Hz.
4. Press A1 key, adjust trimpot W for 221Hz.
5. Repeat steps 3-4 until waveforms are stationary on both keys.
6. With RANGE set in 2', press A3 key and adjust L for 3536Hz.
7. These trims interact to each other, repeat steps 3-6 until three notes are on the right frequency.

## 7-1. ENV-1 S OFFSET

MODULE CONTROLLER (CON)

Applicable to the PCB equipped with VR9



This adjustment must be followed by para. 7. See appendices for adjustment locations and glossary.

1. Connect scope to CON TP-7.

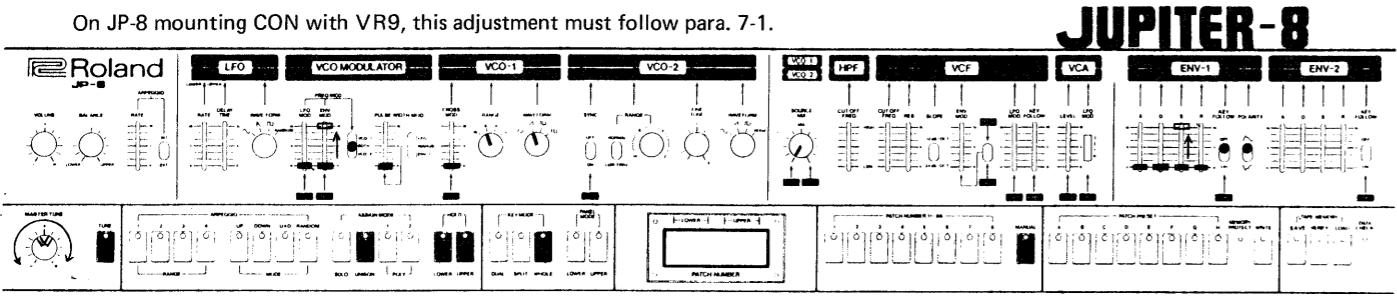
Set scope V to 20mV/div.

2. Adjust CON VR9 for 0V reading.

## 7. VCO ENV MOD BAL

MODULE (MOD)

On JP-8 mounting CON with VR9, this adjustment must follow para. 7-1.



See appendices for adjustment locations and glossary.

1. Push TUNE.
2. Connect scope to MOD TP-4 with A-442 reference to H IN.
3. Press A2 key, adjust MASTER TUNE for still Lissajous.
4. Slide MOD ENV up to 10. Without additional keying, adjust MOD VR8 for still Lissajous. (Frequency is same as in step 3.)

## 8. VCO ENV MOD DEPTH

MODULE (MOD)

This adjustment must follow para. 7. See appendices for adjustment locations and glossary.

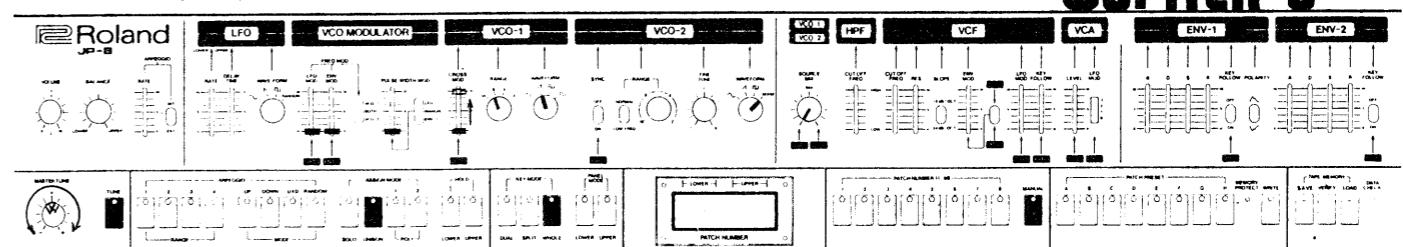
Change from para. 7 setup: ENV-1 S to 10; VCO-1 to 2'; VCO MOD ENV to 0.

The adjustment sets maximum voltage of modulating waveform to the value by which VCO's can be shifted within a 3-octave range.

1. Press A0 key, adjust MASTER TUNE for motionless Lissajous.
2. Set VCO-1 to 16'; VCO MOD ENV to 10. Leaving A0 key open, adjust MOD VR9 for the same waveform as in step 1.

## 9. VCO CROSS MOD BALANCE (X-MOD)

MODULE (MOD) MODULE CONTROLLER (CON)



This adjustment must be followed by para. 10. See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4 with A-442 reference fed to H IN. Place a ground to CON TP-4 or D-20. Push TUNE.

2. Press A2 key, adjust MASTER TUNE for still Lissajous.

3. Leaving A2 key open, set VCO-1 CROSS MOD to 10.

Adjust MOD VR10 for the same Lissajous displayed in step 2.

## 10. VCO CROSS MOD DEPTH (X-MOD LEVEL)

MODULE (MOD) MODULE CONTROLLER (CON)

This adjustment must follow para. 9. See appendices for adjustment locations and glossary.

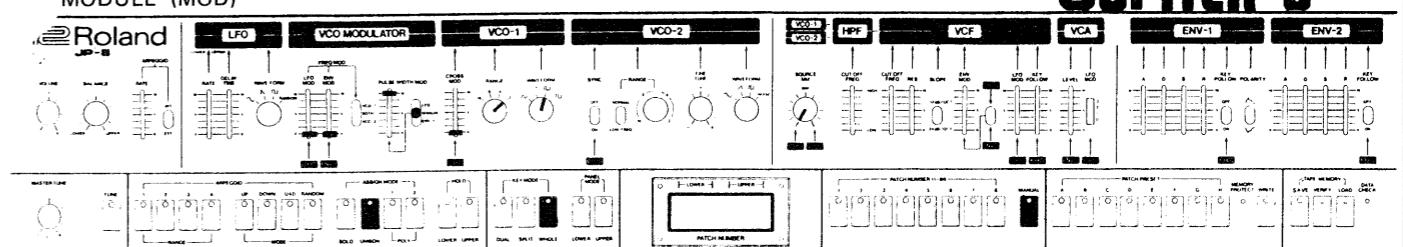
The adjustment sets modulating voltage to the value by which VCO-1 frequency is shifted by 3 octaves when CROSS MOD is set at 5, and VCO-1 RANGE at 2'.

Change from para. 9 setup: VCO-1 CROSS MOD to 5; VCO-2 SYNC to on; VCO-2 RANGE to LOW FREQ.

1. Press A0 key, adjust MASTER TUNE so that Lissajous is 1:1.
2. Switch VCO-2 WAVE to square; VCO-1 to 16'. Adjust MOD VR11 to display Lissajous observed in step 1.

## 11. PULSE WIDTH MOD LEVEL (P.W.M.)

MODULE (MOD)



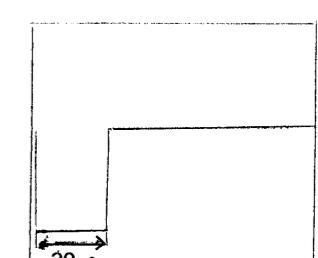
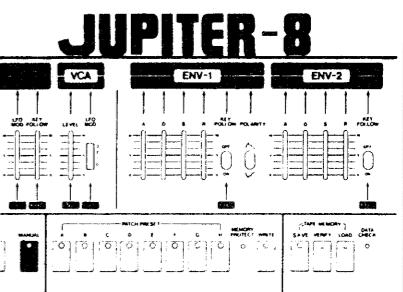
On JP-8's S/N \*\*0600 and subsequent, waveform is up side down.

See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4 or R130 lead. Trigger on the negative edge (positive S/N \*\*0600).
2. Press C2 key, adjust MOD VR12 for 30μs space width.

NOTE:

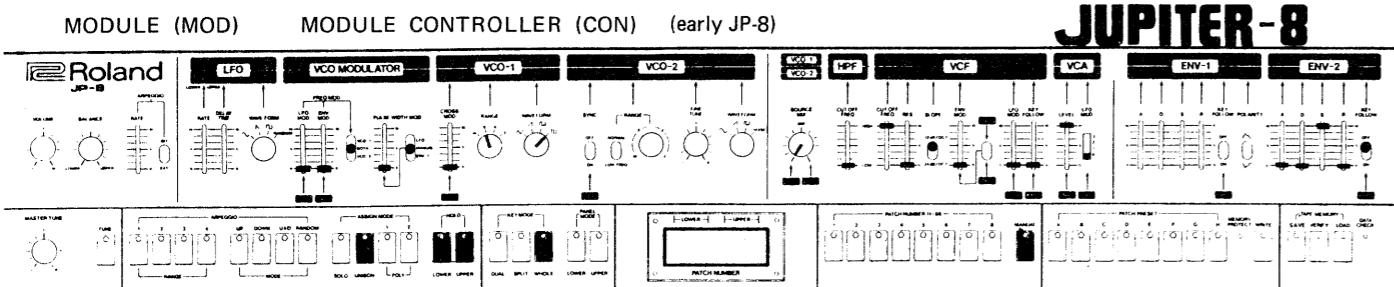
VR12's interact to each other. Check other voices for mark/space ratio. Readjust as necessary.





## 18. VCA LEVEL

MODULE (MOD) MODULE CONTROLLER (CON) (early JP-8)



See appendices for adjustment locations and glossary.

Although CON VR5 is included in part 1, the trimpot is replaced by 10k resistor on later products.

When adjusting MOD replacement, ignore VR5 trimming, following Part 2.

Connect scope to TP-6 or R166 lead.

## PART 1

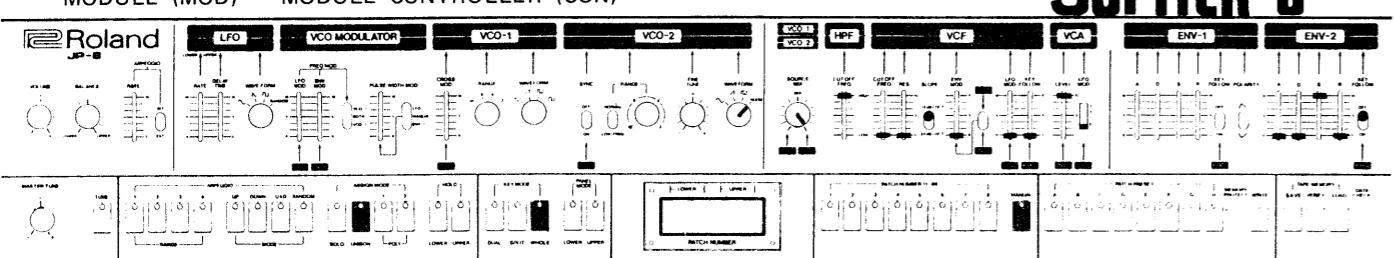
1. Set MOD VR18 wiper to midpoint.
2. Press C2 key and adjust CON VR5 for 3V p-p.
3. Adjust VR18 of the remainder Voices for 3V p-p.

## PART 2

1. Press C2 key and adjust VR18 for 3V p-p.

## 19. VCA BALANCE

MODULE (MOD) MODULE CONTROLLER (CON)

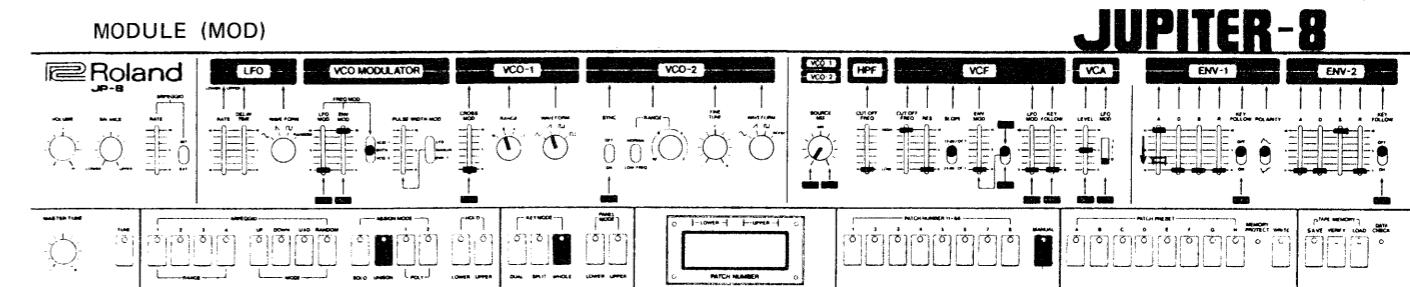


See appendices for adjustment locations and glossary.

1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166. Switch scope to DC coupling, vertical range to 20mV/div.
3. While tapping a key, adjust VR17 so that DC variations are minimized.

## 20. ENVELOPE TOTAL TIME

MODULE (MOD)

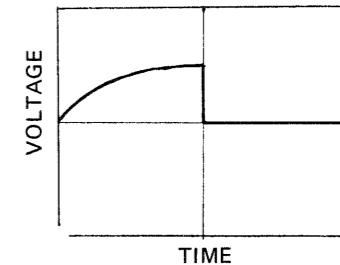


See appendices for adjustment locations and glossary.

This adjustment proceeds on the assumption that all VOICES' ENVs are unadjusted. When adjusting particular module, start from step 3 with scope V IN connected to TP-8 of well calibrated module.

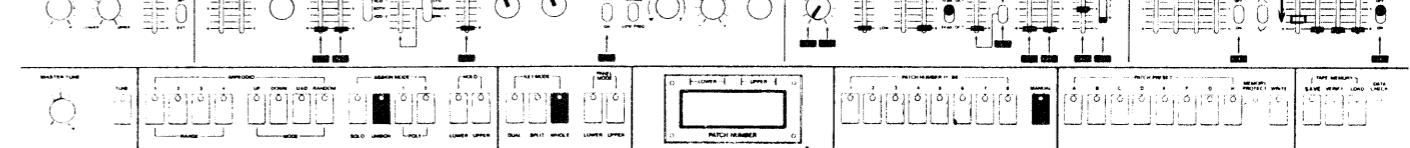
## ENV-1

1. Connect scope to MOD GH R183B lead or TP-8B.
2. While holding a key, time Attack period on scope. Adjust MOD H VR22 for 6-sec attack period.
3. Switch scope timebase to 20ms/div. Trigger scope from TR16 collector of any module.
4. Press and hold a key repeatedly, adjust both ENV-1 ATTACK (around 4-5) and timebase VARI or vernier so that envelope's falling edge is centered on the screen.
5. Shift V lead to TP-8 of the module to be adjusted. Adjust the VR22 for centered falling edge.



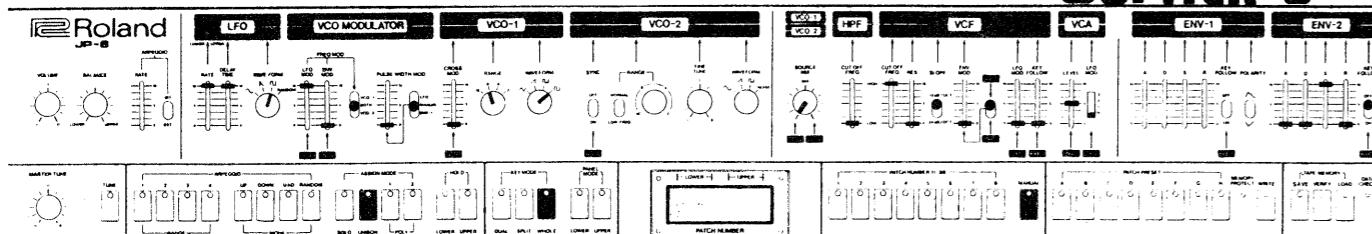
## ENV-2

The procedure is similar to those in ENV-1, but connect scope to R189 lead or TP-7 and adjust ENV-2 ATTACK and VR23.



## 21. LFO MODULATION

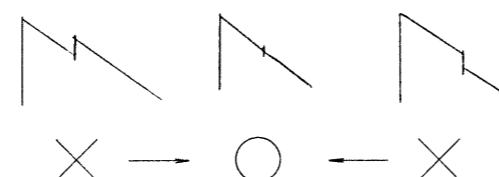
MODULE (MOD) MODULE CONTROLLER (CON)



See appendices for adjustment locations and glossary.

1. Connect scope to CON TP-5 Or R59 lead. Set timebase to 10ms/div.
2. Adjust CON VR3 to display exactly 3 complete cycles on the scope.
3. Adjust CON VR2 for slope straightness as shown in Fig. right.
4. Shift scope to TP-4 of (Upper – MOD A; Lower – MOD E).

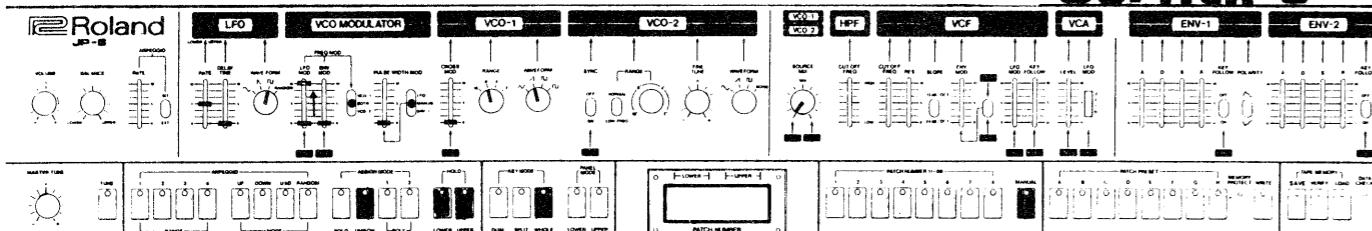
Repeatedly holding a key, adjust CON VR8 so that VCO becomes being modulated approx. 4 sec after the key first depressed.



See appendices for adjustment locations and glossary.

## 22. VCO LFO MODULATION

MODULE (MOD) MODULE CONTROLLER (CON)

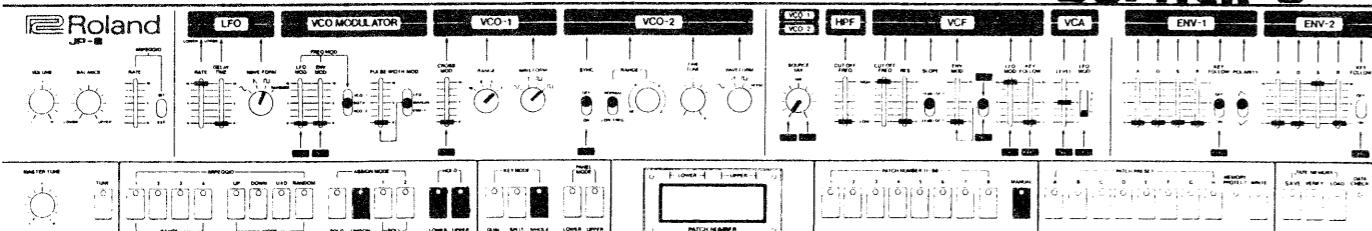


See appendices for adjustment locations and glossary.

1. Connect scope (with A-442 into H IN) to TP-4 of (Upper-MOD A; Lower – MOD E).
2. Press A2 key, adjust MASTER TUNE for 1:1 Lissajous.
3. Set VCO LFO MOD to 10. Lissajous ratio is now changing up and down in sympathy with LFO rate. Adjust CON VR6 so that Lissajous becomes 2:1 at the highest pitch. Note that LFO modulated VCO swing equals 2 oct's.

## 23. VCF LFO MOD LEVEL

MODULE CONTROLLER (CON)



See appendices for adjustment locations and glossary.

1. Connect scope to TP-6 of (Upper – MOD A; Lower – MOD E).
2. Press C2 key (S/N \*\*0600— C4 key), adjust CON VR7 for 50 percentage modulation.



## 24. NOISE

MODULE CONTROLLER (CON)

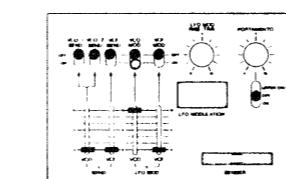
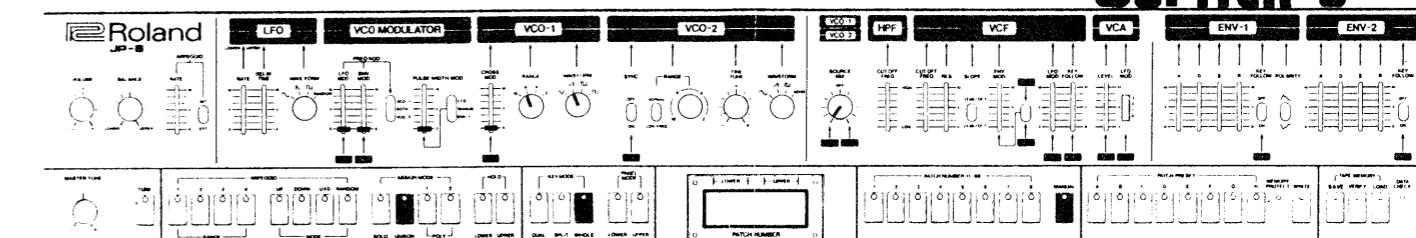
NORMAL RANGE LOW FREQ

See appendices for adjustment locations and glossary.

1. Switch VCO-2 RANGE to NORMAL. Connect scope to CON TP-4.
2. Adjust CON VR1 so that dense signal peaks are approx. 5V p-p.
3. Switch RANGE to LOW FREQ, check peaks for clip.



## JUPITER-8

25. BENDER OFFSET  
BENDER MODULE (MOD)

See appendices for adjustment locations and glossary.

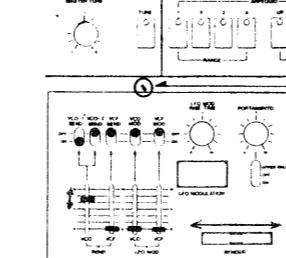
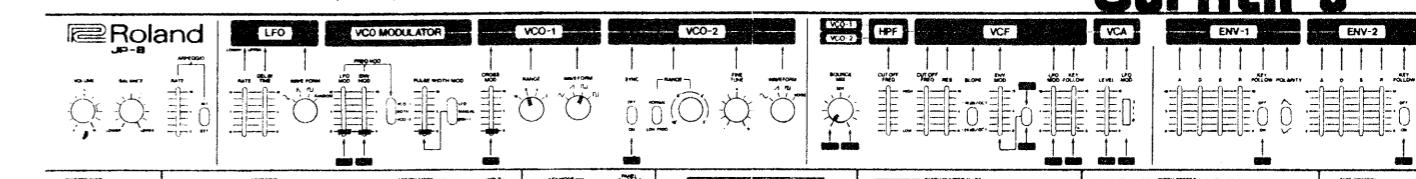
1. Connect scope to TP-4 of (Upper – MOD A; Lower – MOD E) with A-442 reference to H IN.
2. Press A2 key, adjust MASTER TUNE for stationary Lissajous.
3. Set VCO MOD switch to on, adjust VR1 (Upper) or VR2 (Lower) for stationary Lissajous.

NOTE: On JP-8 S/N \*\*0700—, next comes para. 25-1, BENDER LEVEL.

## 25-1. BENDER LEVEL

BENDER MODULE (MOD)

APPLICABLE S/N with \*\*0700 and SUBSEQUENT



## VR3 BENDER ADJ

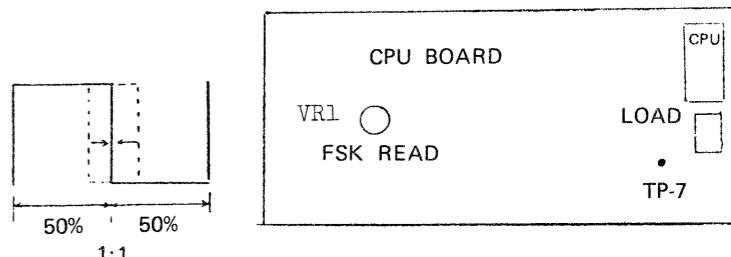
1. Connect scope to TP-4 of any MOD. Press A2 key, adjust timebase and vernier (VARI) to display one complete cycle.
2. Press A3 key. Sway and hold BENDER Lever at extreme left, adjust VCO BEND to display 1 cycle.
3. Press A1 key. Sway and hold BENDER at extreme right, set VR3 for complete 1 cycle.

## 26. FSK

CPU

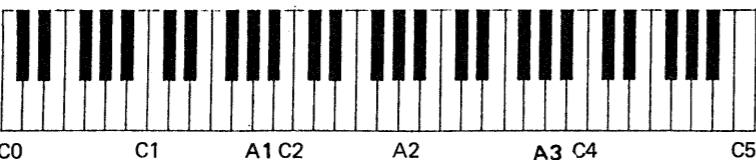
See appendices for glossary.

1. Join TAPE MEMORY LOAD and DUMP jacks via cable.
- NOTE: DUMP is renamed as SAVE on later products.
2. Connect scope to CPU TP-7.
3. Push VERIFY. Be sure that the JP-8 is in test mode, this is displayed in PATCH NUMBER window as —I—I—I—.
4. Set CPU VR1 for 50% duty cycle.
5. Push VERIFY again at the end of adjustment.



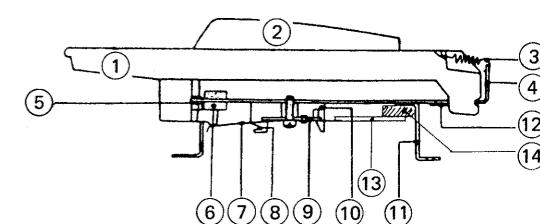
## APPENDIX I

CIRCLED NUMBERS AROUND  
PCB LAYOUT CORRESPOND  
TO PARAGRAPH NUMBERS



## PARTS LIST

CHASSIS	PCB	15189117	TL081CP	OP amp	POTENTIOMETER	POSISTOR	
061H117	Chassis H117 (main)	149H121	CPU board OPH121	151891180A	TL082CP (selected)	SLIDER	560 ERS-B33G561
061H118	Chassis H118 (power trans)		(etch mask 052H267)		13339414 LFE9R-C16A55 (500KA)	15229909	
061H116	Chassis H116 (jack)	149H122	INTERFACE board OPH122	15229801	IR3109 VCF	15229910 1.2K ERS-B33G122	
063H040	Plate (side panel) H40 (right)		(etch mask 052H268)	15229807	IR3R01 ADSR	15229911 1K TSP102J	
063H041	Plate (side panel) H41 (left)	149H123	MODULE CONTROLLER OPH123	15229802	BA662A or B VCA	ARRAY	
PANEL			(etch mask 052H269)	152298020A	BA662A (VF selected) white dot only	13339413 LFE9R-C16B54 (50KB)	
		149H124	MODULE board OPH124	152298020B	BA662A (Offset selected) color dot	13359302 MFE9R-C16B54 (50KB x 2)	
072H078	Panel H78 (upper)	149H125	(etch mask 052H270)	15169301HO	74LS00 Quadruple 2-input NAND gates	13910106 10K x 6 RM6-103K	
072H079	Panel H79 (bender)		PANEL board A OPH125	15169303HO	74LS02 Quadruple 2-input NOR gates	13829821 10K x 8 RM8-103K	
072H080	Panel H80 (right end block)	149H126	(etch mask 052H271)	15169304HO	74LS04 Hex inverters	13910105 22K x 8 RM8-223K	
HOLDER			PANEL board B OPH126	15169341	74LS14 Hex schmitt-trigger inverters	13219811 GM70R-K20AC54P (50KAC)	
064H055B	Holder H55B (pot-pcb)	149H127	(etch mask 052H272)	15169311HO	74LS74 Dual D-type flip-flops	13219812 GM70R-K20B54P (50KB x 2)	
064H092	Holder H92 (key sw)		PANEL board C OPH127	15169313HO	74LS86 Quadruple 2-input exclusive-OR gates	13219225 VM10R-K20B14 (10KB)	
064H100	Holder H100	149H128	(etch mask 052H273)	15169318HO	74LS138 3-line to 8-line decoders	13219243 VM10R-K20C54 (50KC)	
064H101	Holder H101		PANEL board D OPH128	15169319HO	74LS139 Dual 2-line to 4-line decoders	13219231 VM10R-K20A55 (500KA)	
064H094	Holder H94	149H129	(etch mask 052H274)	15169342	74LS156 Dual 2-line to 4-line decoders	13229131 VM10A-K15B54 (50KB CT)	
KEYBOARD			PANEL board E OPH129	15169321HO	74LS161 Synchronous 4 bit binary counters	POWER TRANSFORMER	
004H008	SK-361C	149H130	(etch mask 052H275)	15169322HO	74LS174 Hex D-type flip-flops	022H039J 100V	
KNOB		149H131	PANEL board F OPH130	15169323HO	74LS175 Quadruple D-type flip-flops	022H039C-A 117V	
016-078	Knob NO. 78	149H132	(etch mask 052H276)	15169343	74LS240 Octalbuffers/line drivers with 3-state outputs	13639942MO ECEA-1HN010S 1μ 50V bi-polar	
016H004	Knob H4		BENDER board OPH132	15169331XO	74LS244 Octalbuffers/line drivers with 3-state outputs	13569575FO CQ09S-1H-10000-J5 1000PF styrol	
12479703	KT3-2 (key top) (ivory)	149H139	(etch mask 052H277)	15169324CO	74LS245 Octal bus transceivers with 3-state outputs		
SWITCH		146H059	LEVEL SELECT board OPH139	15169325CO	74LS273 Octal D-type flip-flop		
13149103	2Wi XII (115V) power sw	146H061	(etch mask 052H30)	15169327HO	74LS367 Hex bus drivers	244021500 SN8D500	
13149104	2Wi II (220V) power sw	146H062	POWER SUPPLY board A PSH059	15169329HO	74LS393 Dual 4-bit binary counters		
SLIDE SWITCH			(etch mask 052H302)	15169101XO	7400 Quadruple 2-input NAND gates		
13159118	SSB 022-12RN	146H060	POWER SUPPLY board B (100/117) PSH061	15169116	7474 Dual D-type flip-flops		
13159117	SSB 023-12RN		POWER SUPPLY board B (220/240) PSH062	15169102XO	7406 Hex inverters with open-collector		
13159116	SSB 042-12PN		(etch mask 052H303)	15169117	7407 Hex buffers/drivers with open-collector		
13159503	SQPR-24-12P		POWER SUPPLY board C PSH060	15219109HO	HA-1755C Precision timer		
DIP SWITCH		13449107	JACK	15159503	* TC40H000P Quad 2-input NAND gate		
		13449123	S-G7630 (mono)	15219105	LM565 Phase locked loop		
			S-G7716 (stereo)	15219118	Am6012A 12-bit multiplying D/A converter		
13169606	J-S8719-02		FUSE				
LEVER SWITCH			GHS 1/4A (CPU board)	15119113	2SA1015-GR TRANSISTOR		
13139136	SLE-622-18P	12559137	MGP0003 (3.0A) prim. 100/117V	15119108	2SA798-G		
13139137	SLE-622-18PS	12559521	CEE T1.6A prim. 220/240V	15119105	2SA733-Q or P, K		
13139135	SLE-623-18P	12559518	CEE T5.0A sec. 220/240V	15119601	2SB605-L		
ROTARY SWITCH			017-163	2SB605-KA	13769161DO 12-bit multiplying D/A converter		
13119301	SRM1034-K15		SEMICONDUCTOR	15119813	2SB754-Y		
PUSH SWITCH			IC (* CMOS)	15129114	2SC1815-GR		
13169601	KHC 11901 w/LED		1515914HO	* TC4052BP	Dual 4-channel multiplexer	13769158DO 2.4K	
			15159131	* TC4053BP	Triple 2-channel multiplexer	13769252DO 2.5K	
			15159128TO	* TC4050BP	Hex buffer non-inverting type	13769159DO 2.7K	
			15159113HO	* TC4051BP	Single 8-channel multiplexer	13769160DO 3K	
KEY SWITCH UNIT			15159115HO	* TC4066BP	Quadruple bilateral switch	13769161DO 3.3K	
13129717	KEH 10003 w/key top KT3-2	15159132	* TC40175BP	Quadruple D-type flip-flop	13769163DO 3.9K		
13129714	KEH10903 switch proper	15179308	uPD2101ALC	1024 bit static RAM	13769165DO 4.7K		
13129719	Guide pin CHC32801A	15179111	uPD780C-1	CPU	13769151DO 1.2K		
2226920800	Cushion rubber CK42602A	15179605NO	uPD2716D	16384 bit erasable PROM	13769153DO 1.5K		
		15179305	uPD444C	4096 bit static RAM	13769157DO 390 Ohm		
BUTTON		15179309	uPD2114C	4096 bit static RAM	13439172 304 Ohm		
		15179110NO	uPD8253C	Triple programmable interval timers	13439173 504-12A		
016H010	white			15019103	1S2473	5274-06A	
016H011	dark blue	15149106	CA3046	15019628	05Z-5.6U	5272-08A	
016H012	orange	15199109NO	uPC78L05	15019629	05Z-6.2L	FCN-724P010-AU/0.L 10pin	
016H013	blue	15189111NO	uPC311C	15012626	05Z-11U	FCN-724P020-AU/0.L 20pin	
016H014	green	15189105	uPC4558C	15019624	1S2-52	FCN-724P040-AU/0.L 40pin	
016H017	yellow	15189132JO	NJM4556C	15029110	GL-3AR1 or TLR124, SLP-135 (LED)	FCN-724P050-AU/0.L 50pin	
016H018	red	15189105XO	TL4558C	15029103	TLR124 (LED)	HA16R-3P (canon)	
		15189116	TL080CP	15029404	LN526RA (LED)	043H007 Switch unit 12P	
		151891160A	TL080CP	15019248	6D4B41 (6A 200V)	043H008 Switch unit 13P	
			(selected)	15019247	GP-30G (Hi-Fi special)	104H029 Busbar holder	
						11 062H024 Chassis bracket	
						12 098H006 Key stopper	
						13 052H283-5 Matrix board	
						14 107H059 Cushion	
						NOTE: Although Roland has employed digit coding, old ones (6 digit and with H) are still applied to some	



NO	PART NO	DESCRIPTION	
1	106H026	Natural key	C F
1	106H027	Natural key	D
1	106H028	Natural key	E B
1	106H029	Natural key	G
1	106H030	Natural key	A
1	106H031	Natural key	C' F'
2	106H032	Sharp key	black
3	070H029	Key spring	H29
4	061H086A	Chassis	H86A
5	068H004	Guide bushing	H4
6	101H141	Level felt	H141
7	071H044	Contact leaf	H44
8	071H051	Busbar 8P	H51
	071H054	Busbar 5P	H54
9	043H007	Switch unit 12P	H7
	043H008	Switch unit 13P	H8
10	104H029	Busbar holder	H29
11	062H024	Chassis bracket	H24
12	098H006	Key stopper	H6
13	052H283-5	Matrix board	H283-5
14	107H059	Cushion	H59

NOTE:  
Although Roland has employed 8-10 digit coding, old ones (6 digit and 6 digit with H) are still applied to some parts.

# JP-8 SERVICE NOTES

## PART 2

The following pages cover the information of Engineering changes and various aspects of JP-8 affected by the changes.

### DESIGNE CHANGES THAT CHANGE FEATURE OF THE JP-8

#### DAC

To have JP-8 more stable in pitch, DAC for KCVs is changed from 12-bit to 14-bit version.

#### KEY SPLIT POINT

To make JP-8 more convenient for the user to play on, key split point becomes under the control of the player.

#### DIGITAL COMMUNICATION INTERFACE OC-8 & DCB

To have JP-8 externally controlled through Digital Data Bus connecting either to digitally operating "musical instrument" or to Analog/Digital Interface Unit (e.g. OP-8 that accepts analog CVs in parallel), Digital Communication Interface Board (DCIB) is built in.

**OC-8:** First, DCIB is named OC-8 and sold as an optional kit.

**DCB:** Second, another version of DCIB, called DCB is incorporated in the later JP-8 as a standard feature.

The above-mentioned changes and other significant changes not found on the First Edition of JP-8 Service Notes are listed on the table right.

### PARTS LIST CHANGE

SEE P. 47

### APPENDIX

SEE PP. 48~50

#### PCB LAYOUTS FOR EARLY 500 JP-8's

#### MODULE BOARD

#### MODULE CONTROLLER BOARD

Not published previously, these drawings will help to trace signal paths on old PCBs.

### CHANGE INFORMATION

EFFECTIVE SERIAL NUMBER	MAJOR CHANGE	PART INVOLVED	REMARKS
Below 171700	OC-8 (OPTION): TEST PRODUCTION built into JP-8 with programmable KEY SPLIT feature	PROM Program (CUP board): IC34-IC36 Version from 1.0 to 2.1	made only on a few JP-8's see table on the next page
171700 181899	D/A CONVERTER... from 12-bit to 14-bit format	INTERFACE BOARD: PCB 052H268 to 052H268 DAC (IC14) from Am6012 to ITS80141 Some ICs and circuits CPU BOARD: PROM programs (IC34-IC36) Version 1.0 to 3.1	14-bit INTERFACE BOARD is compatible with the 12-bit PCB only when PROMs of CPU BOARD are replaced with of version 3.1 or 3.2 see P. 34 for detail
	OC-8 (OPTION): made as a commercially available kit for both 12- and 14-bit versions	ROMs IC34-IC36 of CPU BOARD to be replaced upon installing OC-8	IC34-IC36 must be 3.2 version and are supplied in an OC-8 kit together with PROM IC33 containing communica- tion program
181900	PROMs PROGRAM... revised to be compatible with those stored in OC-8 kit PROMs	CPU BOARD: IC34-IC36 from 3.1 to 3.2 version	additional PROM 3.4D (IC33) only is necessary upon installing OC-8 see table on the next page for detail
202100	MODULATION CIRCUITS: To have U and L sounds kept balanced	MODULE CONTROLLER BOARD: PCB from 052H269 to 052H269 some circuits	when U or L board is replaced with new one, the remainder should be slightly modified. see pp. 36-38 for detail
202210	RAM (MODULE CONTROLLER BOARD IC 49): make equivalent RAM usable	CPU BOARD: IC23	short pin 5 of IC23 to ground see p. 38 for modification
242750	LED DISPLAY: adopt brighter LED	PANEL BOARD F: from LN526RA to LN5620A	new and old LEDs are different in color and brightness mix use should be avoided for uniformity
272850	FUNCTION SWITCH: LED to diffusive, brighter type	PANEL BOARD E: PANEL BOARD G: function switch from KHC11901 to KHC11026 (LED from AR3432S to SEL2210R)	
282880	DCB BOARD (similar to OC-8): built into JP-8 as a standard feature	CPU BOARD MODULE CONTROLLER BOARD PANEL BOARD A	drawings related to this change begin at p. 40

## HOW TO IDENTIFY PROM VERSION

## CPU BOARD

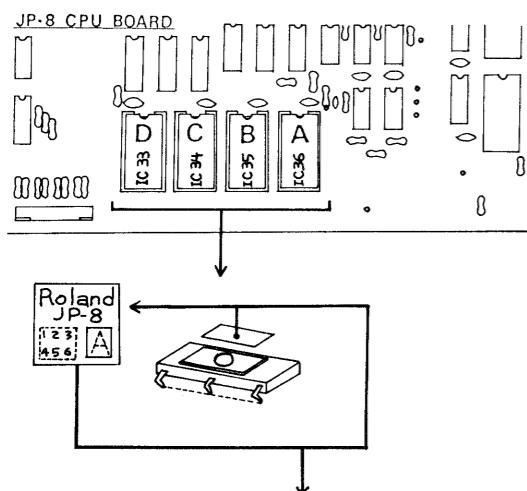
Version is indicated by hand written number or marking on the label as shown below.

Version can be displayed in PATCH NUMBER window (LOWER). Turn the JP-8 on while pressing PATCH NUMBER buttons 1 and 3.

## NOTES:

In 0.7 or 1.0 version, displayed number will change quickly from 07 (10) to 13.

In 3.2 (A, B, C) and 3.3D (3.4) arrangement, number 33 (34) will change to 32 if PROM D is removed.



## PROM VERSION      PROGRAM

0.7 1.0	12-BIT DAC FIXED KEY SPLIT POINT
2.0	12-BIT DAC VARIABLE KEY SPLIT POINT
1) 2.1D	DIGITAL COMMUNICATION INTERFACE
3.1	14-BIT DAC VARIABLE KEY SPLIT POINT
3.2 2) 3.3D (3.4)	14-BIT DAC VARIABLE KEY SPLIT POINT
3.3D (3.4D)	DIGITAL COMMUNICATION INTERFACE

1) This is a special version. Replace each with the same one, or replace all four with a set of 3.2 and 3.4D version.  
 2) Co-operates with 3.3D or 3.4D for Digital Communication Interface.

When need arises to modify the JP-8 or to replace parts:  
 First consult the table below, then refer to the right as necessary.

## PROM REPLACEMENT

When replacing PROMs A, B and C with different version, replace them in a set.

Version 3.2 can replace 3.1, 1.0 and 0.7

Version 3.1 can replace 1.0 and 0.7

The reverse does not hold true.

ROM 3.4 can replace 3.3D and vice versa.

## NOTES:

PROM D is required only when OC-8 or DCB BOARD is present.

PROM D must be used together with A, B, C of 3.2 version and up.

PROM D contains diagnostic programs.

Refer to P.46 for test procedure.

Difference between 3.3D and 3.4D is that the latter has debugged diagnostic program.

INTERFACE BOARD ..... p. 34  
 MODULE CONTROLLER BOARD ..... pp. 37, 38  
 RAM IC49 of MOD CON BOARD ..... p. 38  
 CPU BOARD (in relation to RAM IC 49) ..... p. 38  
 OC-8 ..... OP-8 (OC-8) Service Notes

SERIAL NUMBER	PROM VERSION				DISPLAY	The JP-8 may be or may have	Features of the JP-8	Addable new feature	PROM	VERSION	INTERFACE BOARD w/14-bit DAC	by-product
	A	B	C	D					A, B, C 3.2	D 3.3 or 3.4		
PROTOTYPE	0.7				□ □	as produced	DAC ..... 12-bit KEY SPLIT POINT .... Fix OC-8 ..... less	DA ..... 14-bit SPLIT POINT ..... Valiable OC-8 ..... built in	●		●	Variable Split point
030100	1.0	123 456	123 56		1 □	as produced	DAC ..... 12-bit KEY SPLIT POINT .... Variable OC-8 ..... built in	DA ..... 14-bit	●	●	●	Variable Split point
171699	123 456	(3.2)	123 456	JP-8 2.1D or 3.3D or 3.4D	2 □	OC-8: installed at the factory	DAC ..... 12-bit KEY SPLIT POINT .... Variable OC-8 ..... built in	DA ..... 14-bit			●	
171700 181899	123 456				3 □	as produced	DA ..... 14-bit KEY SPLIT POINT .... Variable OC-8 ..... less	OC-8 ..... built in	●	●		
181900 282879	123 456				3 □	as produced	DA ..... 14-bit KEY SPLIT POINT .... Variable OC-8 ..... less	OC-8 ..... built in		●		
171700-272829	123 456	(3.2)		3.4D	3 □	OC-8: built in as option	DA ..... 14-bit KEY SPLIT POINT .... Variable OC-8 (DCB) ..... built in					
2828800	123 456					DCB: built in as a standard feature						

When new feature is required, replace existing part(s) with the one indicated by ●.

## INTERFACE BOARD OPH122A

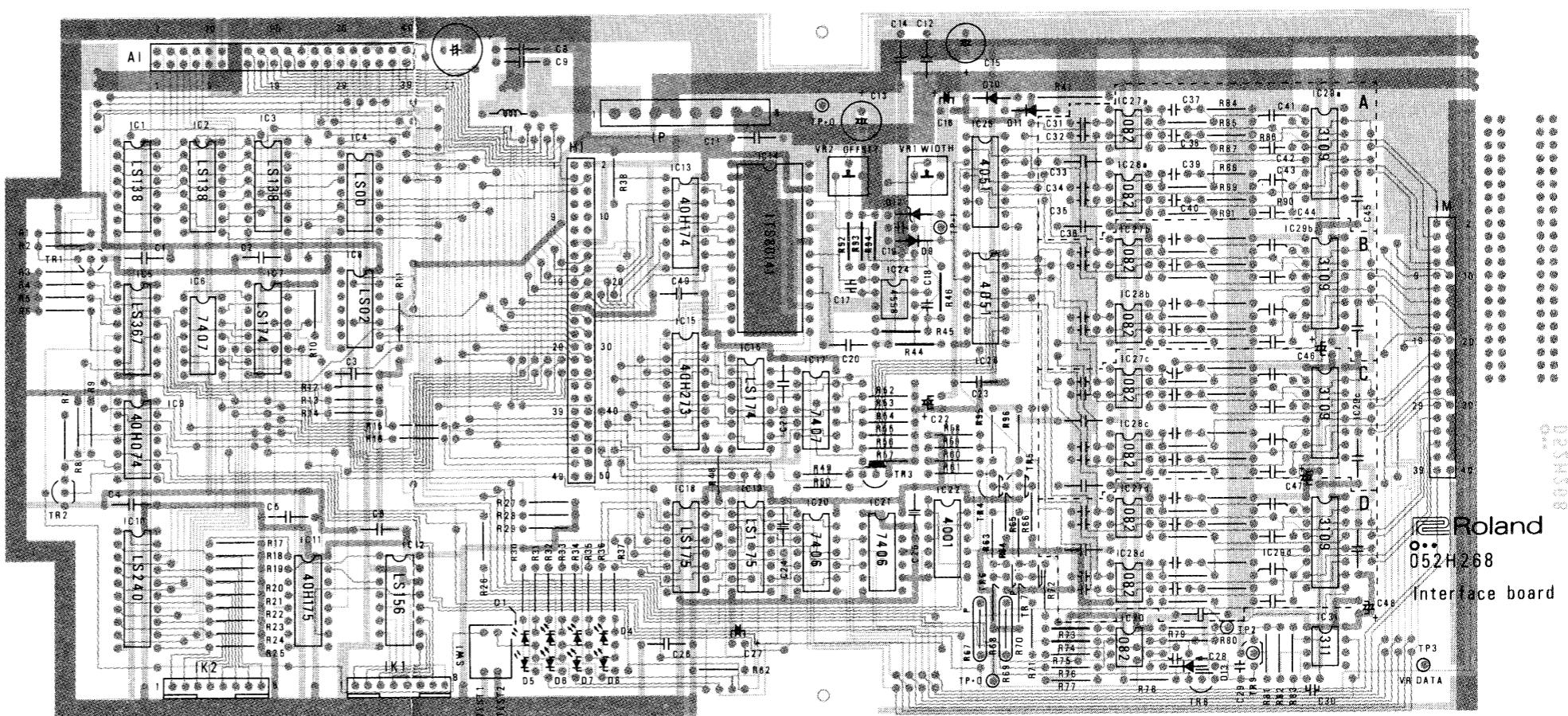
(149H122A) (pcb 052H268)

**SN 171700 and higher**

## MAJOR CHANGES

## D/A CONVERTER ..... 14BIT

## KEY SPLIT POINT ..... PROGRAMMABLE



This board can replace 12-bit INTERFACE BOARD when PROMs of CPU board are of correct version. See right below.

Besides suffix (A, B, etc.), the PCBs occasionally bear marks “●” and/or “○” above its code number to show the edition.

- stands for 1, and ○ for 5.

Example: ○••• = 8th edition

The D/A Converter IC14 is changed from 12-bit Am6012 to 14-bit ITS80141 with this PCB version. Along with the change the following parts are also changed.

PART	From	To
Latch	LS273 (TTL, IC13)	40H273 (CMOS, IC15)
	LS175 (TTL, IC15)	40H174 (CMOS, IC13)
Multiplexer	LS175 (TTL, IC11)	40H175 (CMOS)
Multiplexer	4051 (IC25, IC26)	HD14051 (Hitachi only)
Flip-flop	74LS74 (IC9)	TC4013 (SN212330-UP TC40H74)
Gate	LS02 (IC22)	TC4001

#### Prepare PROMs for CPU board:

A, B, C

3.1 version

or  
3.2 version (inevitable when OC-8 exists)  
for IC34-IC36

D (when OC-8 is built in)

3.3 or 3.4 version for IC33

Replace existing PROMs with these PROMs.

Adjust DAC circuit, referring to "4. DAC" on p.25 of this book.

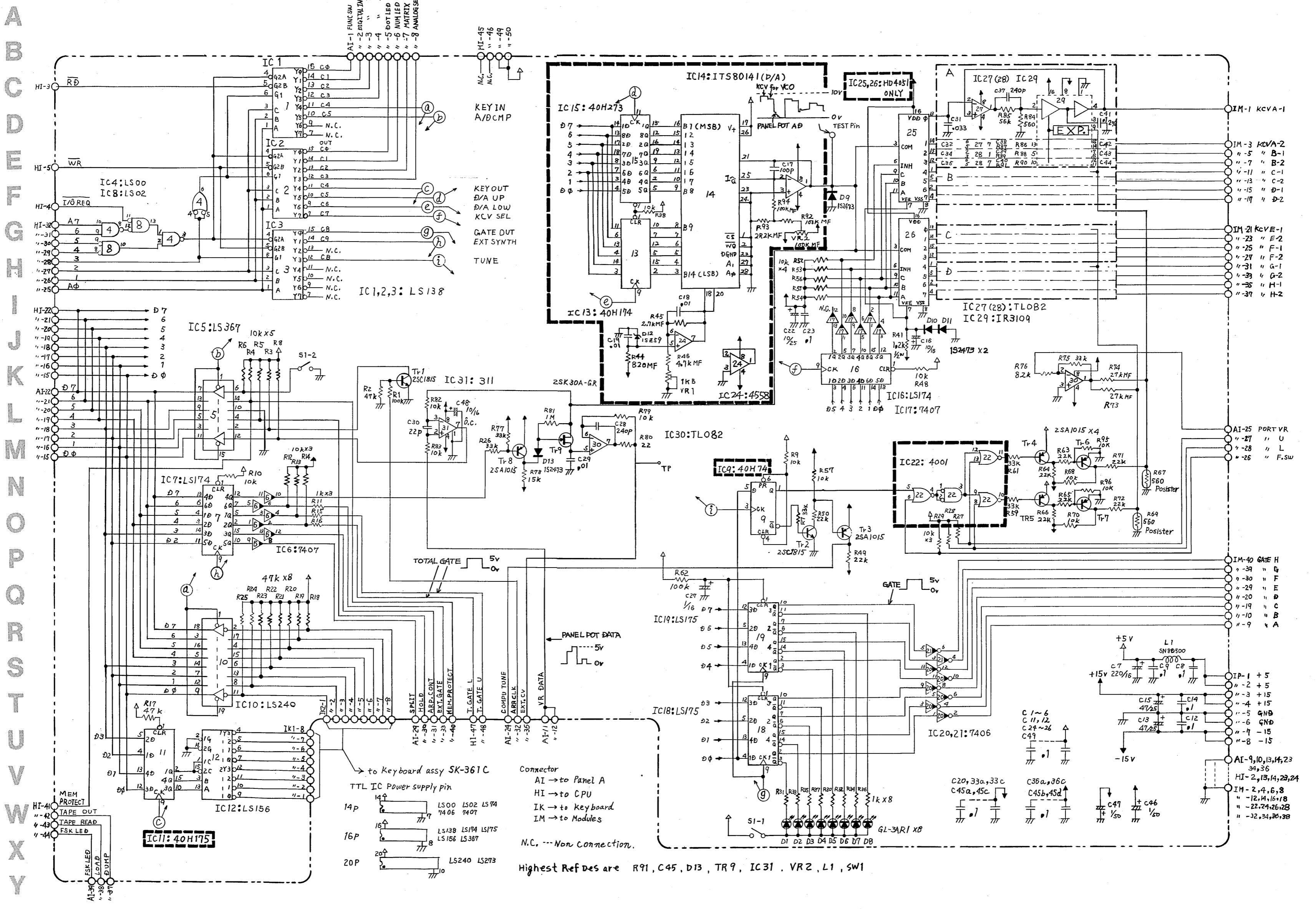
**NOTES:**

This interchange does not affect adjustment procedures except that the letter "PLL" are displayed in PATCH NUMBER window after —|—|—| during FSK adjustment steps.

At the end of Computune cycle(s), defective VCO that has not "tuned-in" is indicated in MANUAL and PATCH- NUMBER or PRESET buttons.

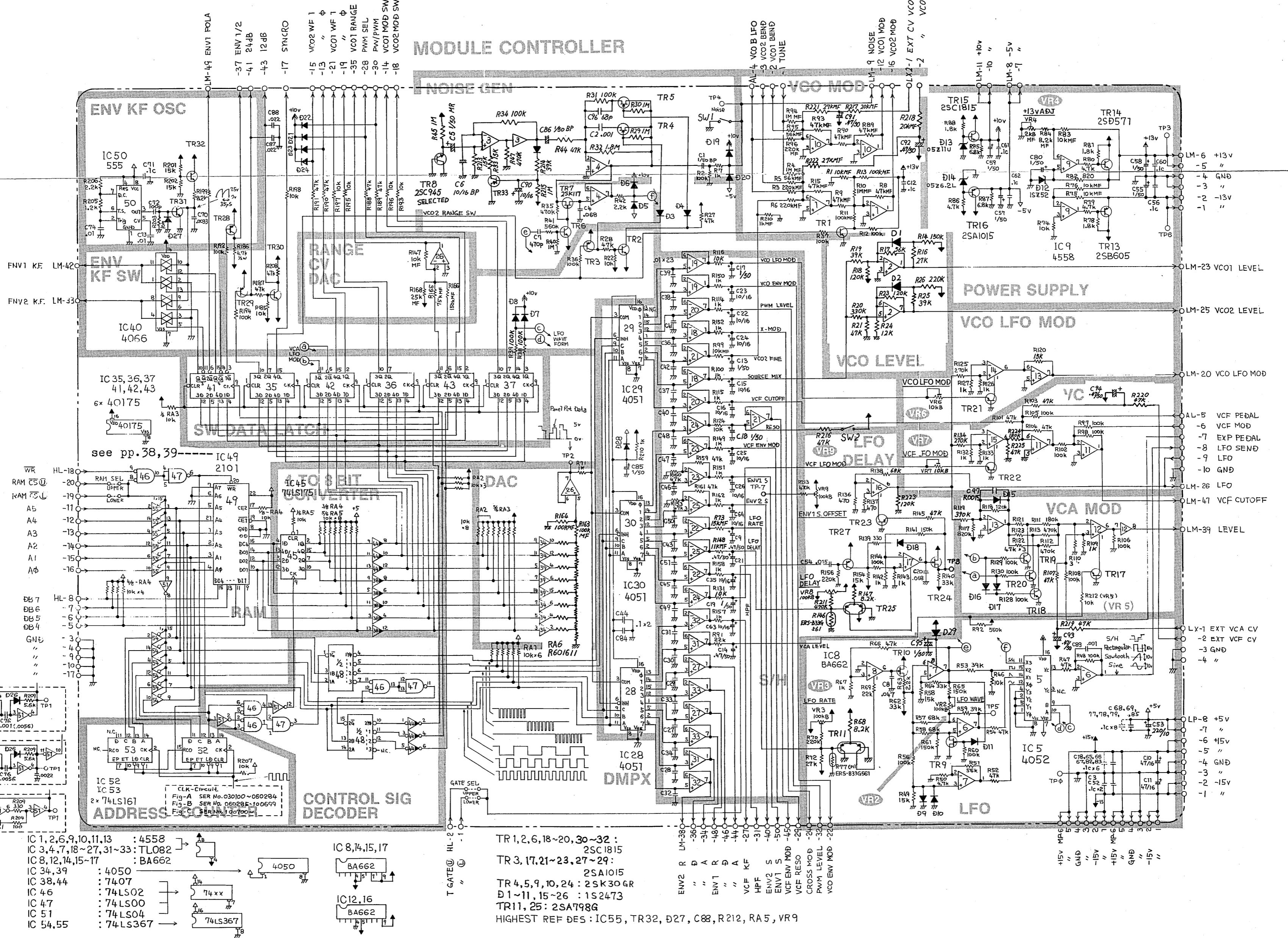
See p.39 for indicators and difference in computuning between 12-bit and 14-bit systems.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47

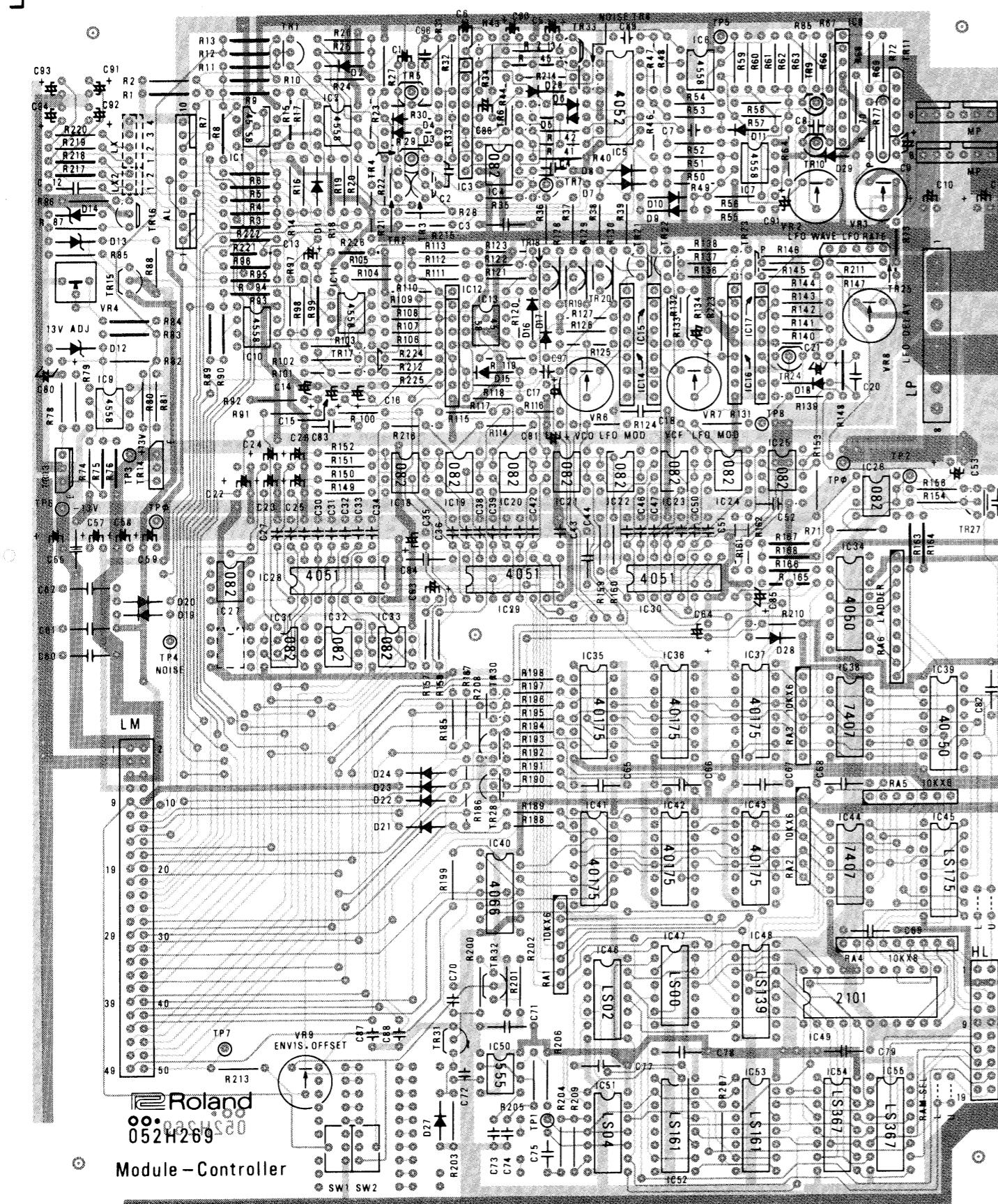


2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 4

A  
B  
C  
D  
E  
F  
G  
H  
I  
J  
K  
L  
M  
N  
O  
P  
Q  
R  
S  
T  
U  
V  
W  
X  
Y  
Z



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

**MODULE CONTROLLER BOARD SN 202100 and UP****OPH123A (149H123A) (pcb 052H269)****IMPORTANT**

When replacing MOD CON BOARD or RAM IC49,  
SEE PAGE 38 (P.48 for early 500 units).

**CHANGE INFORMATION**

(Each heading is followed by address to the circuit diagram.)

**1. NOISE GENERATOR (D-H, 18-27)**

IC3: from TL082 to BA662 having AGC.  
NOISE LEVEL VR1: omitted

**SAMPLING SIGNAL**

Previous circuit:

Only white noise is routed to S/H circuit regardless of VCO-2 RANGE position.

New circuit:

Pink noise is selected for S/H when RANGE is in LOW position.

**2. D/A CONVERTER (O-R, 23)**

Ladder Resistors: from discrete to resistor array

**3. NOISE KILLER SWITCH (D-E, 28)**

Newly attached for cutting off noise signals. Used in particular adjustments. Close this switch when step states "Place a ground to MOD CON TP-4".

**4. RESONANCE SWITCH (M,33)**

To emphasize regeneration to the point of oscillation. Used for factory adjustment only.

**5. LFO DELAY CONTROL (R, 33)**

From TR25 and TR26 to single paired-transistor TR25 to have U and L delay times synchronize with each other.

**6. LFO RATE (V,33)**

From TR11 and TR12 to single paired-transistor TR11. To minimize speed difference between U and L LFOs.

**7. Add D29 and C95 to +B pin of IC7 (S, 36) to stabilize the supply voltage****8. Add RC filters on EXT CV lines (L, 43; S, 41; E, 35; D, 33)**

To filter out noise induced into EXT CV.

**9. VCO LEVEL (J, 33-34)**

Apply a ground to pin 5 of IC2 through R21, previously -15V. Change resistors values in this section

To set VCO-1 and VCO-2 audio levels to an equal amount when SOURCE MIX is set at 12 o'clock position.

To have the same volume changes in VCO-1 and VCO-2 sounds, that is, the change in volume of VCO-1 when SOURCE MIX is being rotated toward VCO-1 is the same as that of VCO-2 when S.M. being toward VCO2.

**10. VCA MOD (O, 38-39)**

Add C97 across pins 1 and 2 of IC13  
To eliminate click noises at positive or negative going transient.

**11. Add TP-8 (Q, 36-37)**

For factory adjustment only.

**IC49, RAM 2101 and 5101**

SN 202210-UP

Often, RAM 2101 is substituted by 5101 upon manufacturing or shipping replacement because of procurement problem.

RAMs of these models have different characteristics in timing response.

To make both RAMs compatible, factory modification on CPU board started with above Serial number. (See p.38 for detail.)

**NOTE:**

Beside suffix (A, B, etc.), the PCBs occasionally bear marks "o" and/or "o" above its code number to show the edition o stands for 1, and o for 5. example: o... 8th edition.

# GUIDES ON REPLACEMENT

## MODULE CONTROLLER BOARD

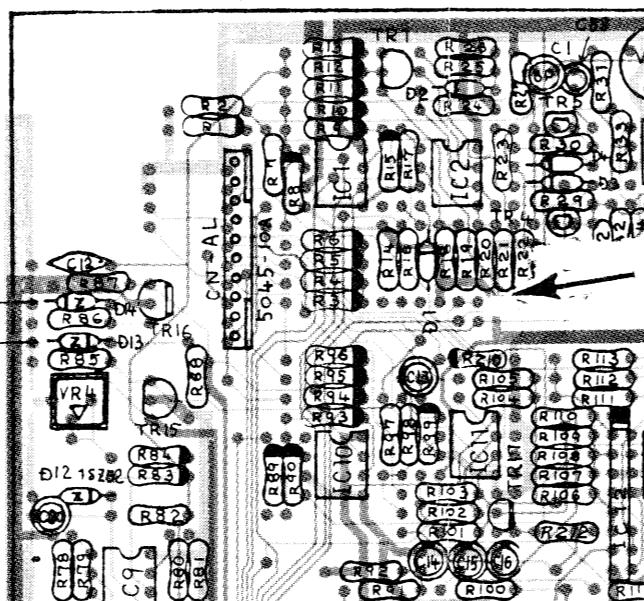
(For early 500 units, see p.48)

When replacing OPH123 with OPH123A, be sure to proceed the following.

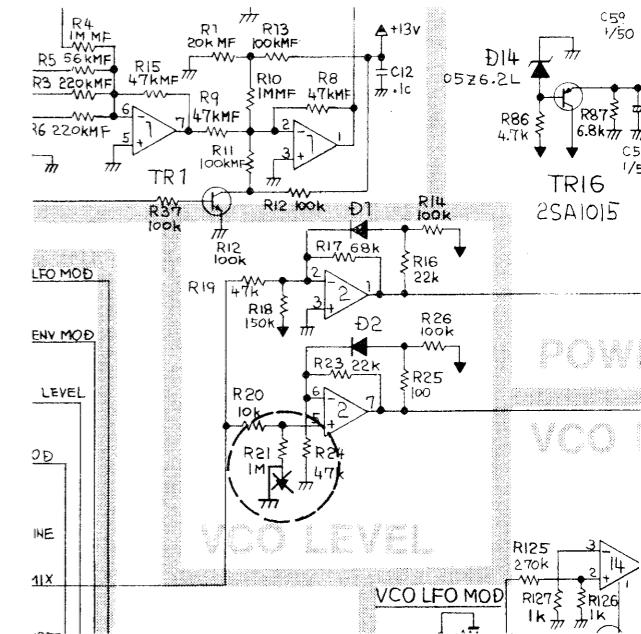
Check IC49 on the both PCBs (being replaced and replacement) for name. If 2101 is on the existing PCB and 5101 on the replacement, take the modification illustrated below.

When replacing Upper board or Lower only:

Adjust VR1 (NOISE LEVEL) of unchanged MOD CON board to match the noise level of new board which omits the adjustment. Reconnect R21 of unchanged MOD CON, referring to drawing to the right. This will eliminate possible loudness differences between U and L voices.



Disconnect R21 lead at negative end and solder it to the nearest ground foil.



Factory modification SN 202210-UP

## IC49 OF MOD CON BOARD (MODIFICATION ON CPU BOARD)

(RAMs 2101 and 5101)

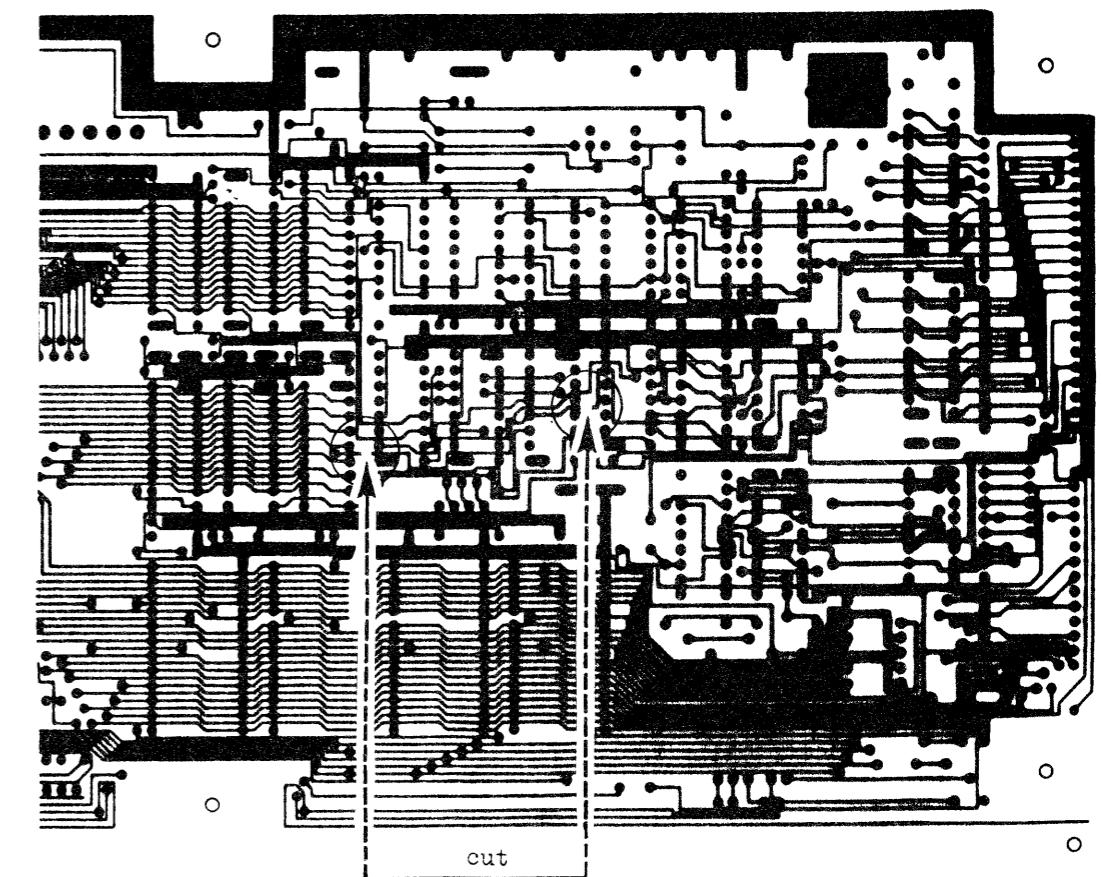
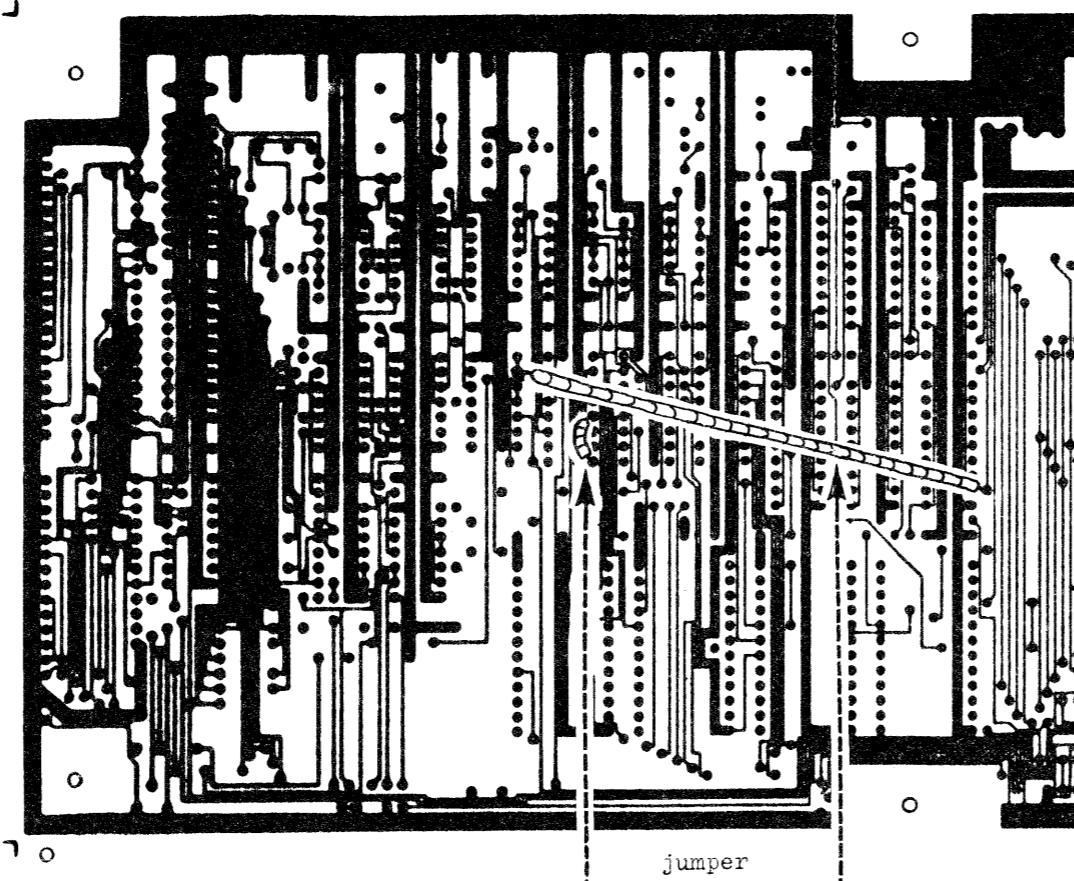
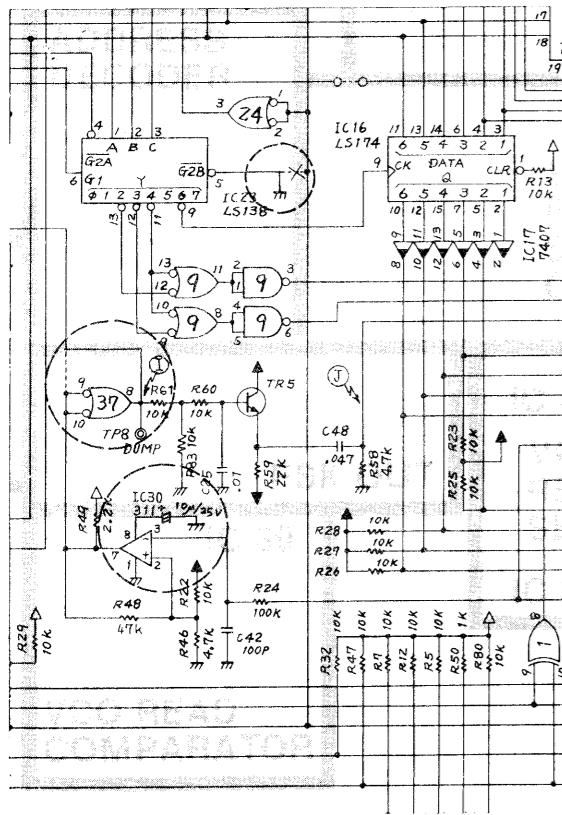
Below, two minor modifications (independent of RAM change) are also indicated:

Reconnection of IC37 and addition of 10UF at IC30  
pin 8

Insertion of 5101 into a place previously occupied by 2101 requires pin 5 of IC23 on CPU board to be grounded. This reconnection as illustrated is to protect the data on panel control from garbled – while a control is being reset, some of other controls

are also detected as moving; in extreme case no voice would sound. This is due to the fact that two RAMs differently respond to the same timing signal.

This modification has no adverse effect on 2101.



## CIRCUIT DESCRIPTION

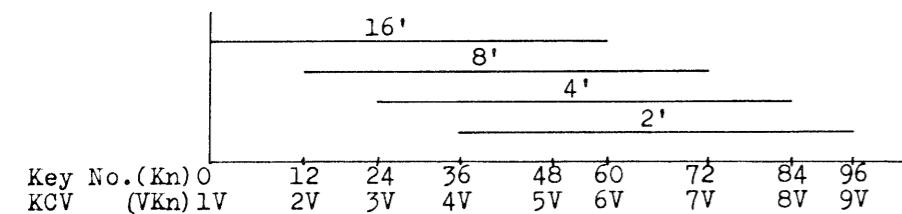
This circuit description applies to the JP-8 with serial numbers 171700 and up where DAC changed from 12- to 14-bit version, and concentrates on computune program which is revised in line with the change.

This description makes reference to pages 6 and 7 "WIDTH" and "KCV" of the Circuit Description of First Edition issued separately.

## WIDTH

P. 6 Change title to WIDTH & TUNE

The coverage of the JP-8 keyboard is expandable to 96 keys using footage selector (RANGE SWITCH). In the following, KCV and key designation are defined as below.



In this mutual arrangement any KCV (VKnx) at a key (Knx) is obtained from the equations:

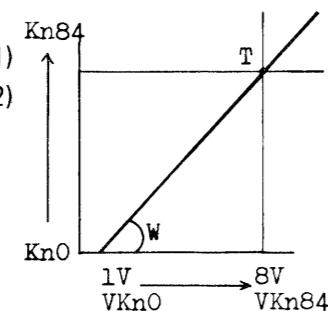
$$\text{VKnx} = \text{VKno} + W(\text{WIDTH}) \times \text{Knx} \quad (1)$$

$$\text{or} \quad \text{VKnx} = T(\text{TUNE}) - W(84 - \text{Knx}) \quad (2)$$

where,  $W = 1/12(\text{V})$

— voltage steps per half tone

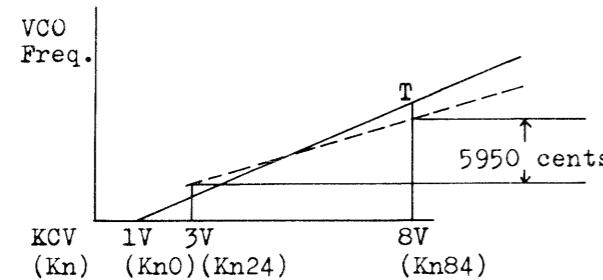
$$T = \text{VKn}84$$



In the following computuning, T is a reference voltage in calculating every KCVs to the equation (2) above.

Upon power on for the JP-8, computune program starts frequency measurements at two points with MOD.A VCO-1 by applying KCV of Kn24(3V) and VCO Freq. to it. If the VCO output is 20 cents higher than expected pitch at 3V KCV, and 30 cents lower at 8V as shown in the figure right, the factor W is given by:

$$\frac{8 - 3(\text{V})}{9570 - 3620(\text{cent})} = 0.084$$



Substituting 0.084 for W in equation (2) above would provide the VCO with KCVs for every keys, and the VCO will oscillate in 1V/oct steps with most of pitches slightly out of tune.

To bring each note in tune, the program first adds fine tune voltage (bias) ...  $0.084 \times \frac{30}{100}$  (cent) = 0.0252V — to T. Then, finds KCVs for every notes by applying equation (2).

$$\text{Example: } \text{VKn}24 = 8.025(\text{T}) - 0.084(\text{W}) \times (84 - 24) = 2.985\text{V.}$$

When compare this WIDTH with the WIDTH determined by previous 12-bit system, the new system provides more precise resultant because of wider measurement range.

## INITIAL TUNING UPON POWER ON

When the power is first turned on for the JP-8, thermally unstalbe VCO tends to oscillate on frequencies which are greatly deviating from the expected frequency so that computune circuitry will not be able to determine exact pitch error at a time. If a program encounters such a VCO, the program ceases measurement for that VCO but retains the data, then proceeds to the next VCO. After all the VCOs have been measured, the program resumes operation from the first VCO, depending on the previous data. However, the process is repeated only two times per oscillator, regardless of the frequency deviation. Properly functioning VCOs will be brought into tolerance at the second time.

Most VCOs outside tolerances after completion of the second execution might be brought closer and closer to desired pitches if the computune program is forced to repeat the operation by manual triggering of TUNE button. (See next paragraph.)

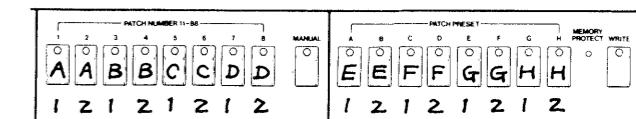
Tuning sequence is visually confirmed on flashing LEDs in the PATCH buttons.

## VCO BEING MEASURED

PATCH NO.	1st cycle		2nd cycle	
	MODULE	VCO	MODULE	VCO
1	A	1	E	1
2	A	2	E	2
3	B	1	F	1
.	.	.	.	.
.	.	.	.	.
8	D	2	H	2

However, when one PATCH LED stays on while MANUAL LED is flashing, they are indicating failure in that VCO. The computune program cannot correct such a VCO as is indicated by a PATCH button as below, and does not proceed to the next VCO unless one of function switches is touched.

MODULE  
VCO



## COMPUTUNE WITH TUNE BUTTON

When the computune program is triggered manually with TUNE button (after power-on-tune), it runs only once for each VCO since the program already had data on fine tune, and drastical change in VCO frequencies is likely to occur. If the program fails to compensate frequency drift, iterative tapping of "TUNE" will bring VCO closer to correct pitch. Relying on this method is preferable only in an emergency; the cause of out of tune must be eliminated as early as possible.

## KCV (INTERFACE BOARD)

P. 7 Lines 9 and 10: Delete

Lines 11-17: Reads as follows.

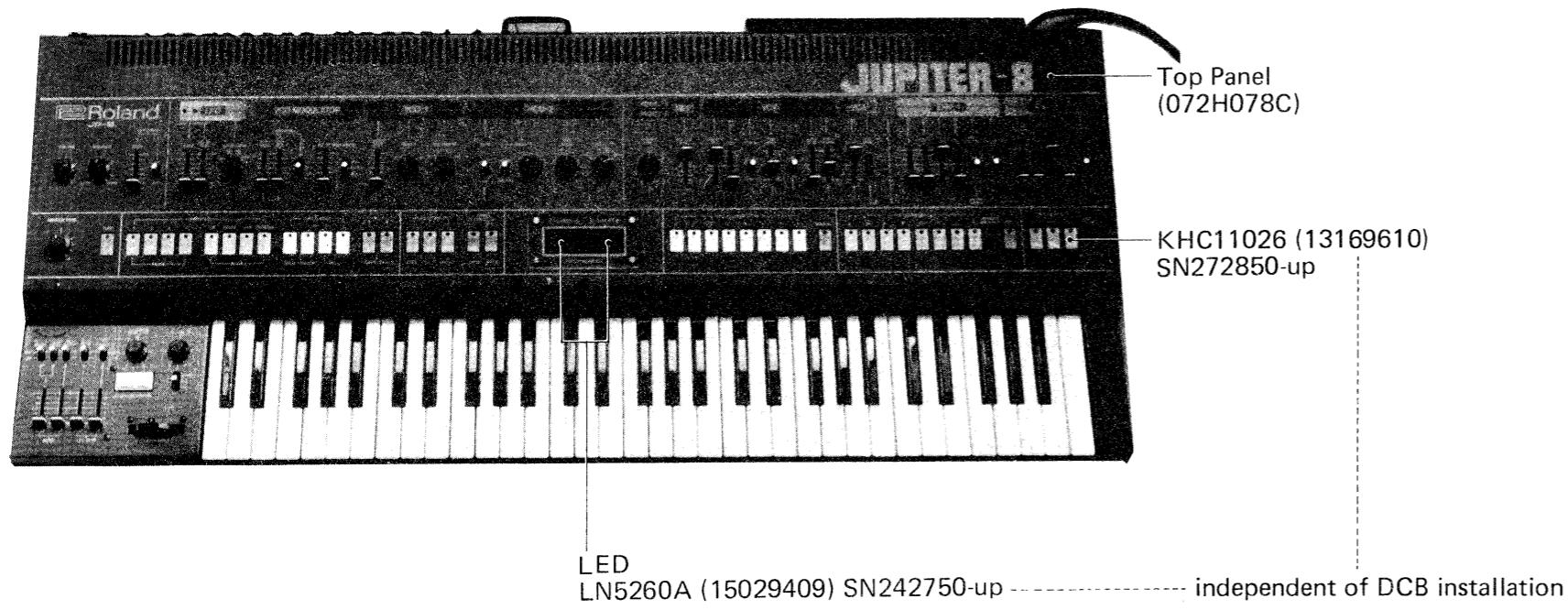
Each KCV data is represented in 14-bit format and is divided into two pieces—MS (most significant) 8-bit is latched by IC15 followed by LS 6-bit into IC13. DAC output has a range of 0-10V against 14 bits, thus resolution is  $10\text{V} \div 2^{14}$  (bit) = 0.6mV, nearly equals 0.7 cents in pitch. During I/V conversion in 1/IC24, CV for EXT. jack is scaled 1V/oct.

## CORRECTION

## CIRCUIT DESCRIPTION

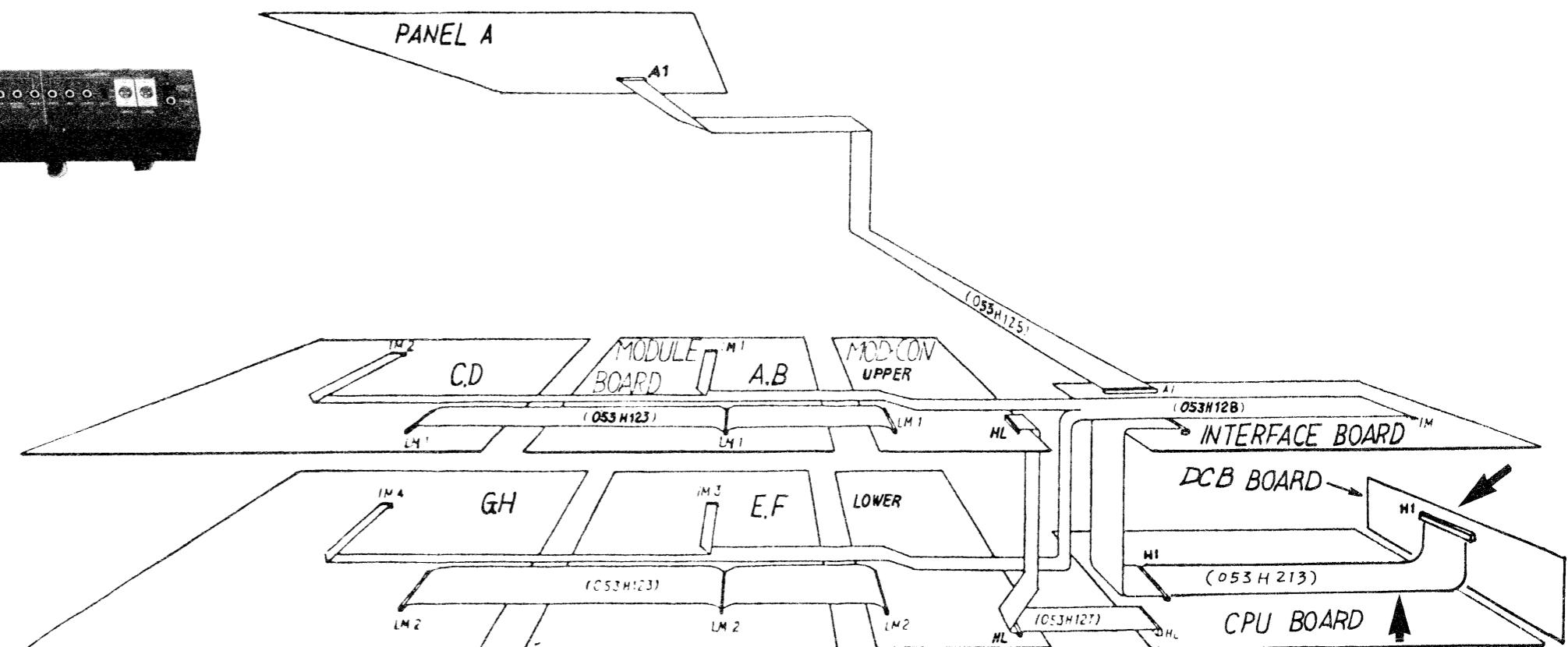
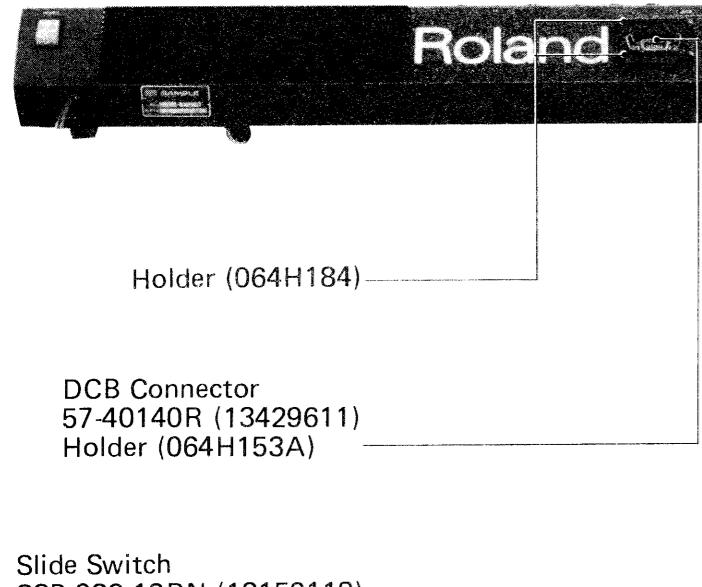
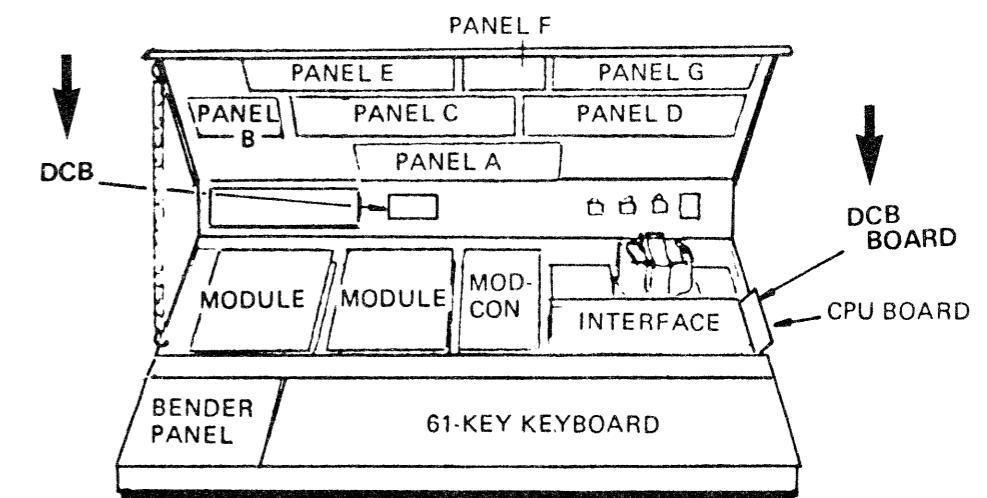
P. 11: PUSH SWITCH SCANNING

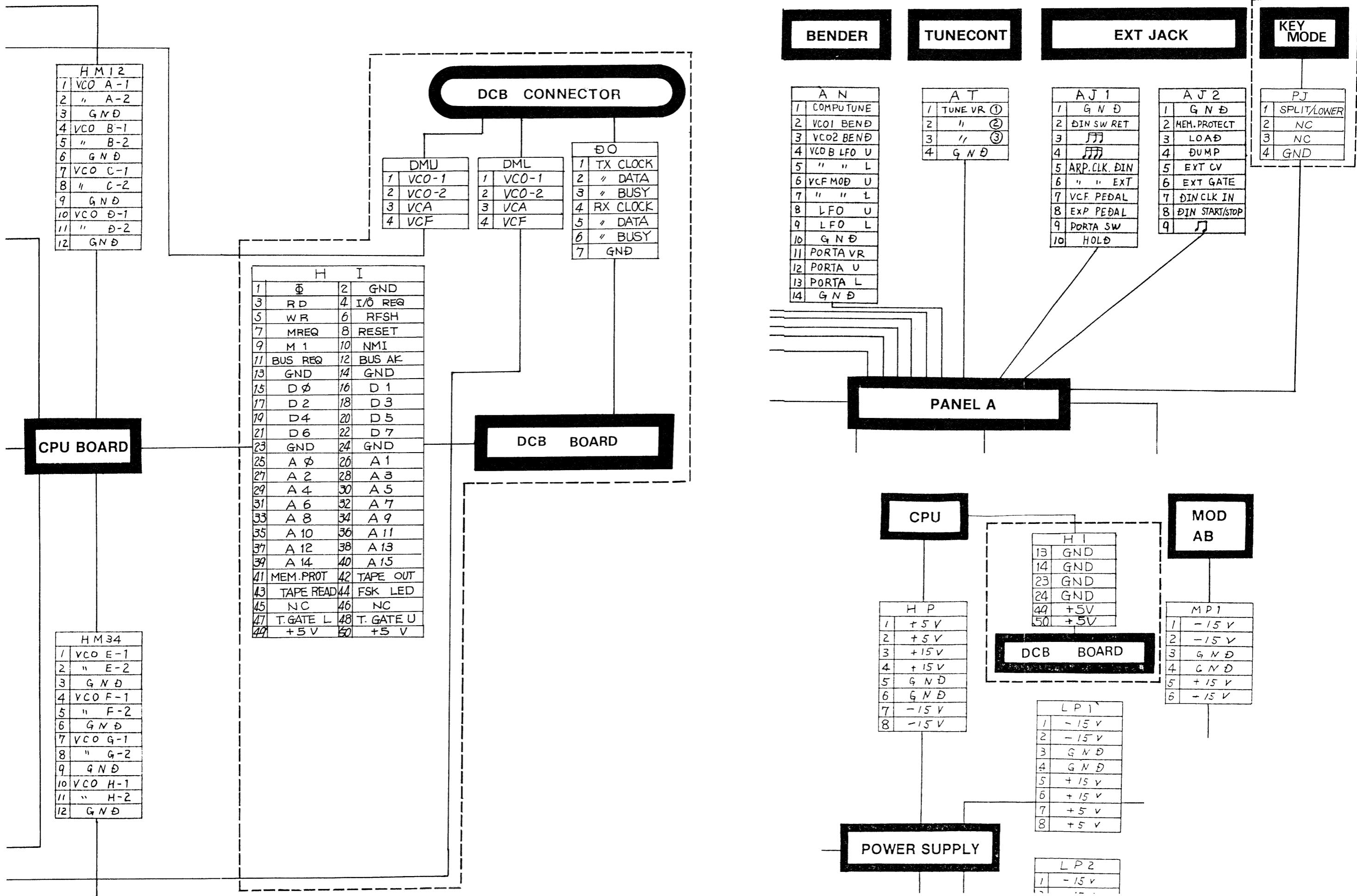
Push switches (function switches with LED) are read every approximately 25ms (not 1ms). See timing chart on page 3 of the Circuit Description. LEDs are lit every 1ms when INT signal is applied from IC26 which in turn is timed by the signal generated at pin 17 of IC40. Failure of INT signal causes no LED driving signal, but has no relation to the switch reading performance.



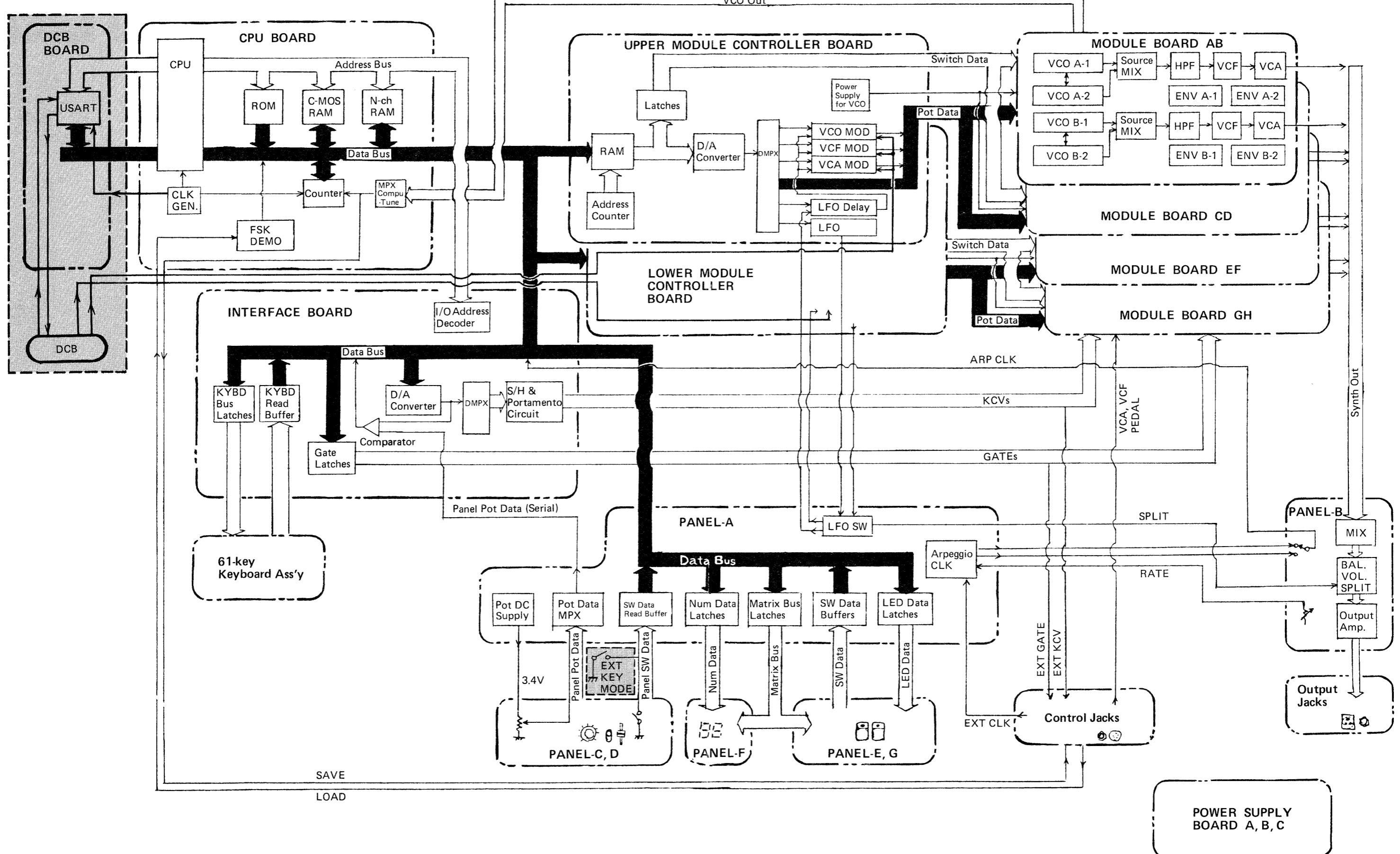
## **CHANGES, MODIFICATIONS, ADDITIONS**

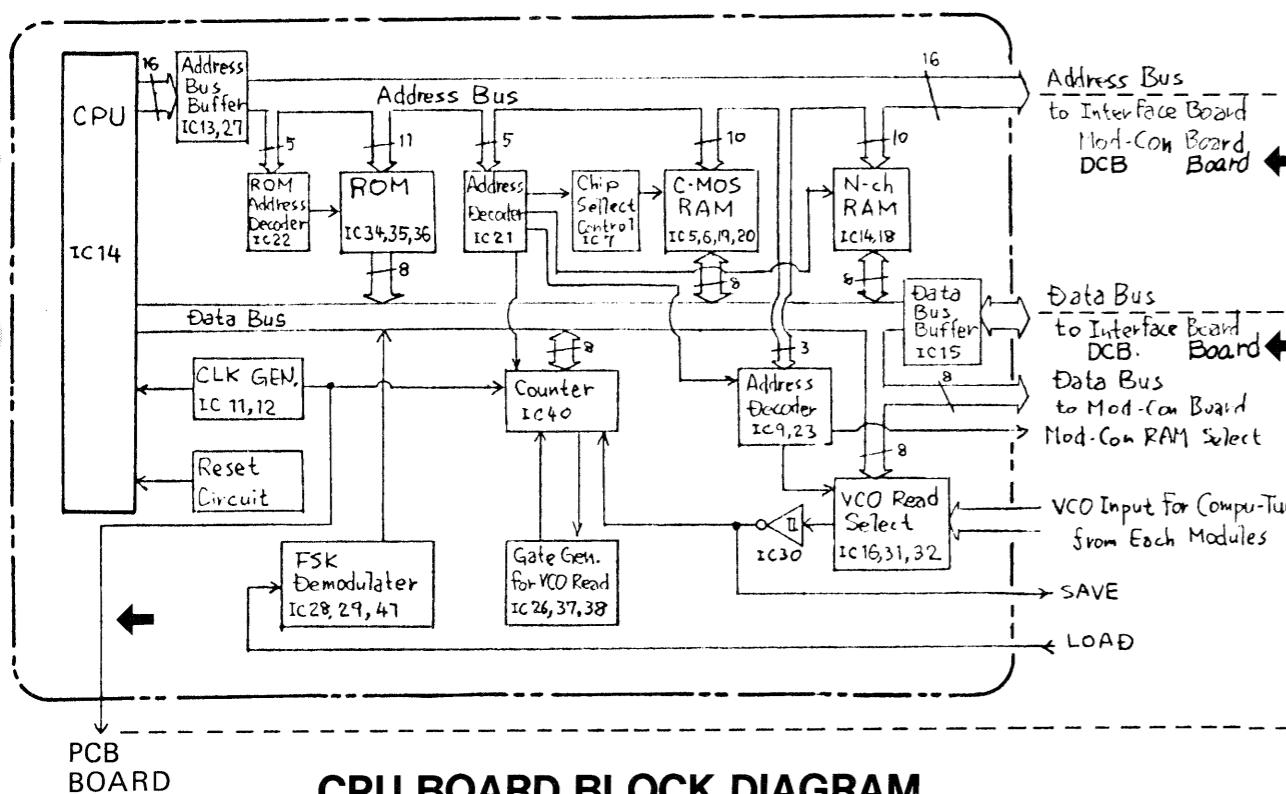
## **INVOLVED IN IMPLEMENTING DCB (Digital Communication Bus) BOARD**



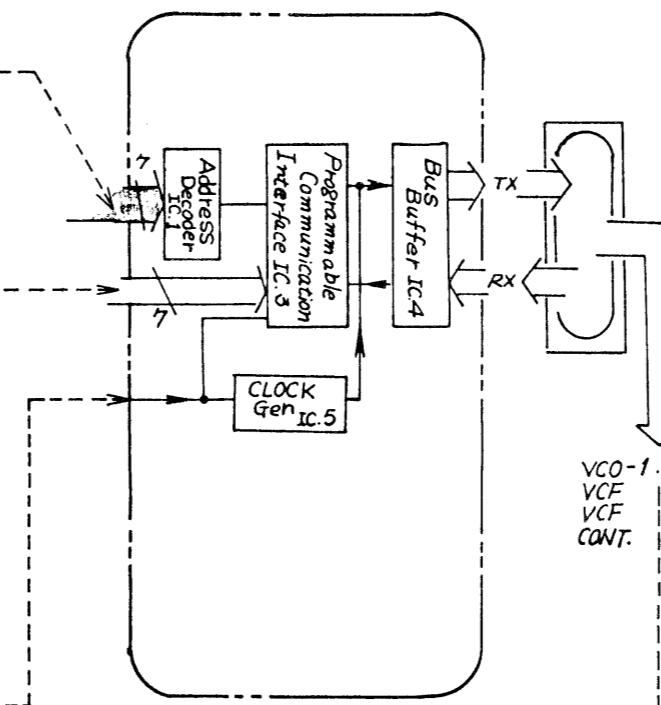


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41

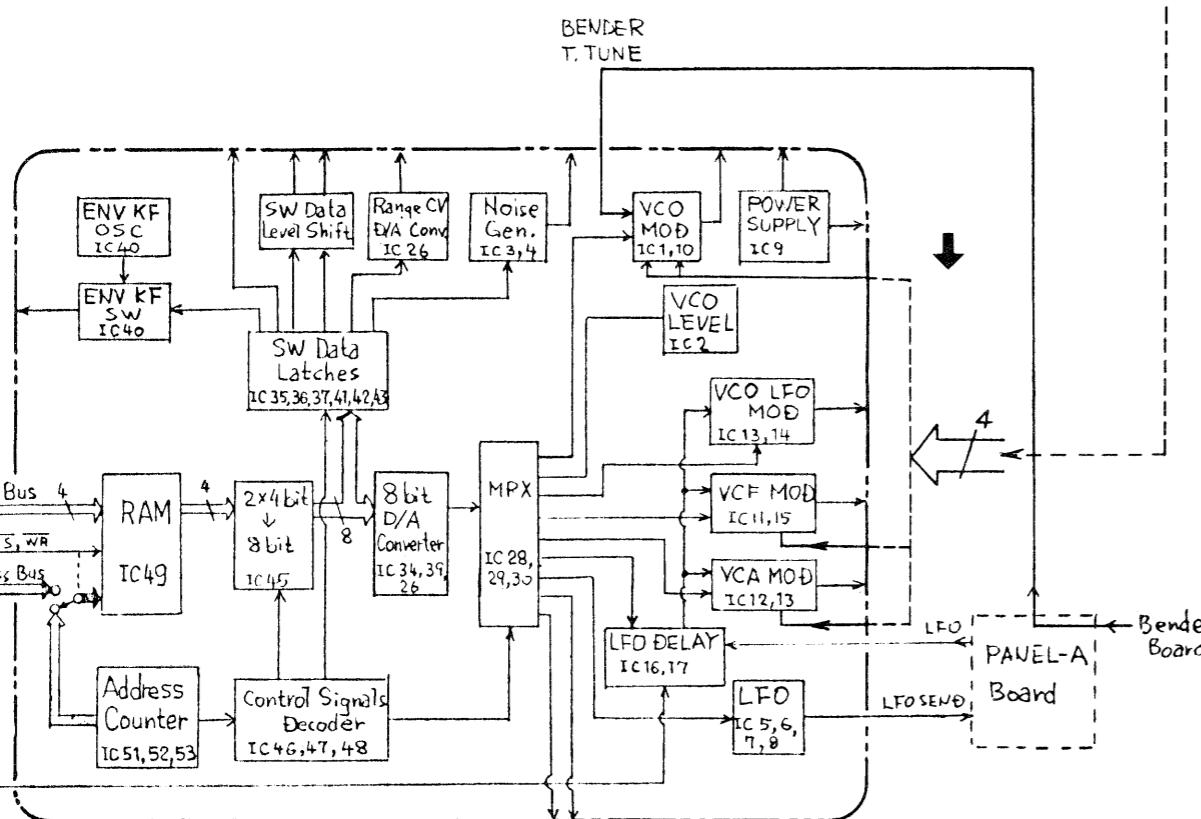
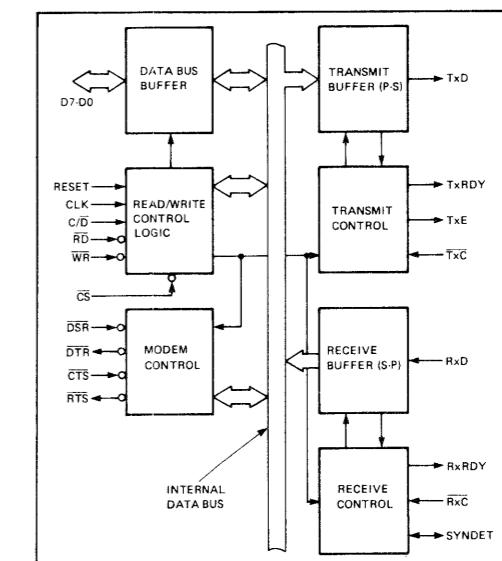




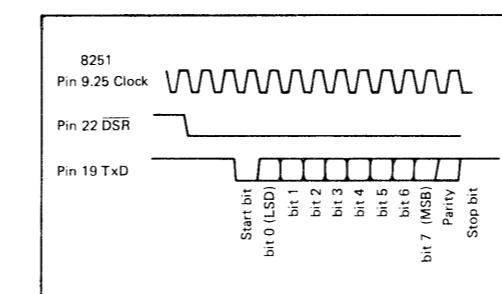
CPU BOARD BLOCK DIAGRAM



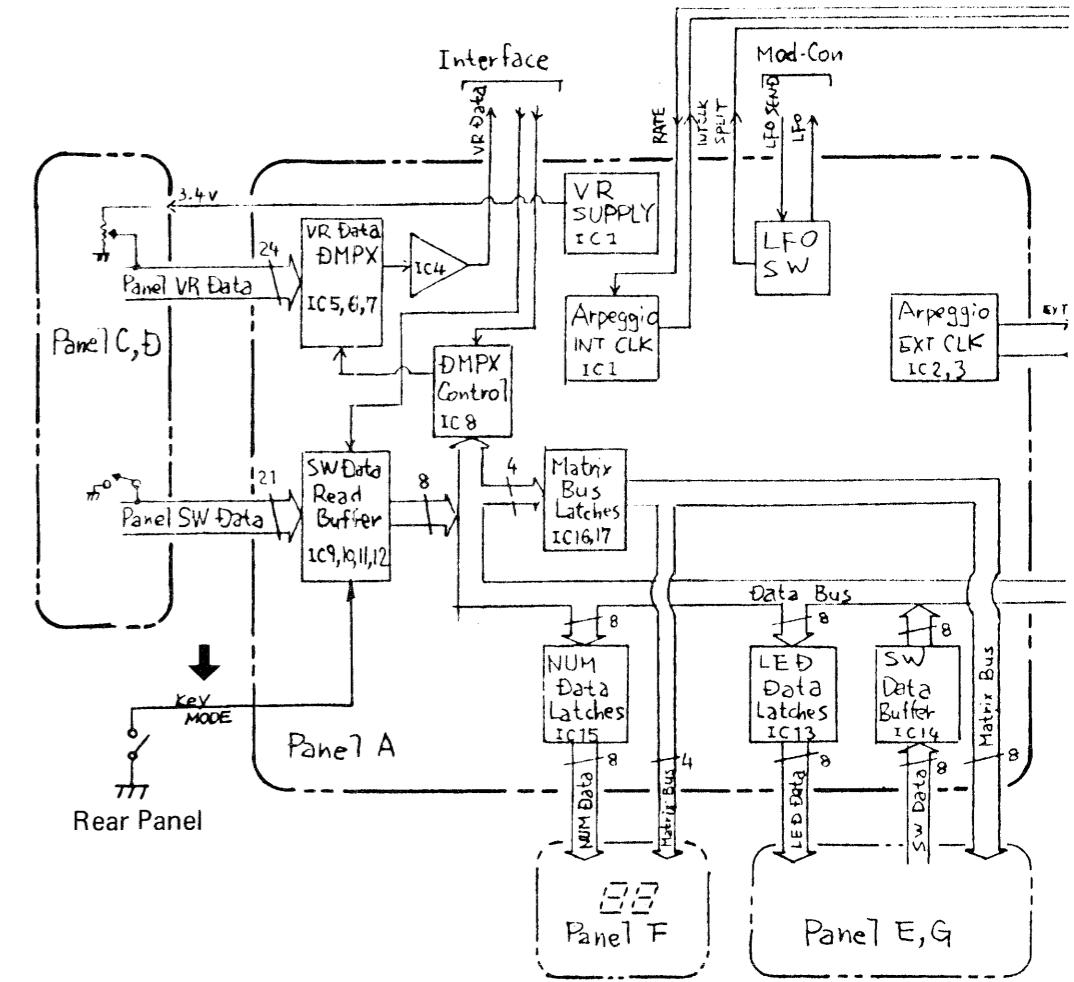
DCB BOARD



MOD-CON BOARD BLOCK DIAGRAM



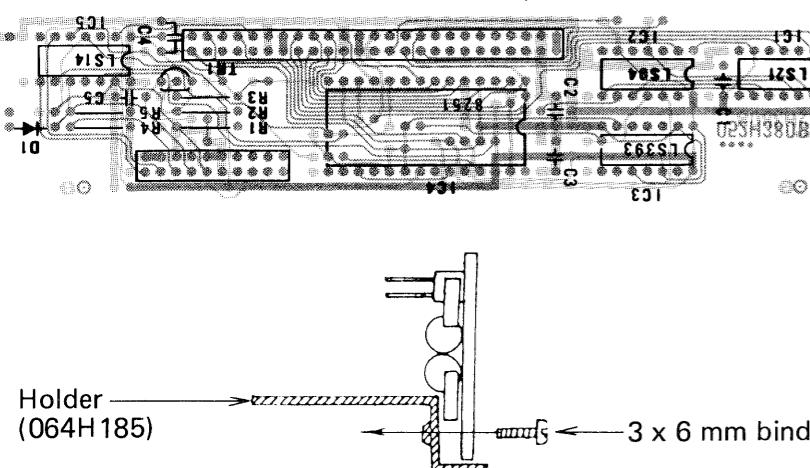
8251	D7-D0	Data Bus (8 bits)
	C/D	Control or Data is to be Written or Read
	RD	Read Data Command
	WR	Write Data or Control Command
	CS	Chip Enable
	CLK	Clock Pulse (TTL)
	RESET	Reset
	TxC	Transmitter Clock
	TxD	Transmitter Data
	RxD	Receiver Clock
	RxRDY	Receiver Data
	TxRDY	Receiver Ready (has character for 8080)
	DSR	Transmitter Ready (ready for char. from 8080)
	DTR	Data Set Ready
	SYNDET/BD	Data Terminal Ready
	RTS	Sync Detect/Break Detect
	CTS	Request to Send Data
	TxE	Clear to Send Data
	V <sub>cc</sub>	Transmitter Empty
	GND	+5 Volt Supply
		Ground



DCB BOARD 6 6 7 6 9 10 11 12 13 14 15 16 7 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42

OPH220 (149H220) (pcb 052H380B)

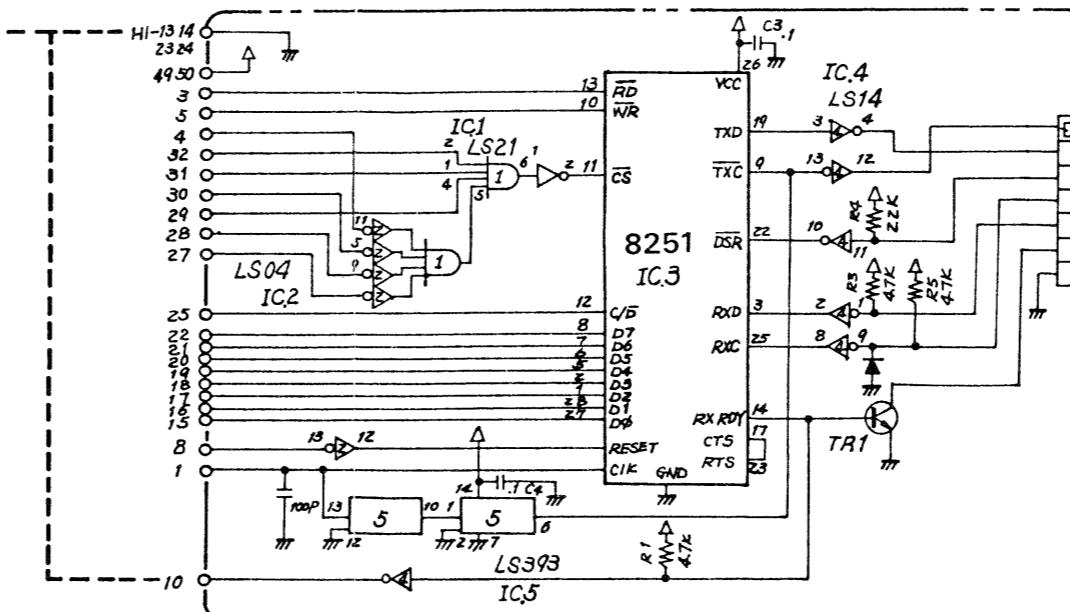
FCN724PC50-AU/L



JP-8

DCB BOARD

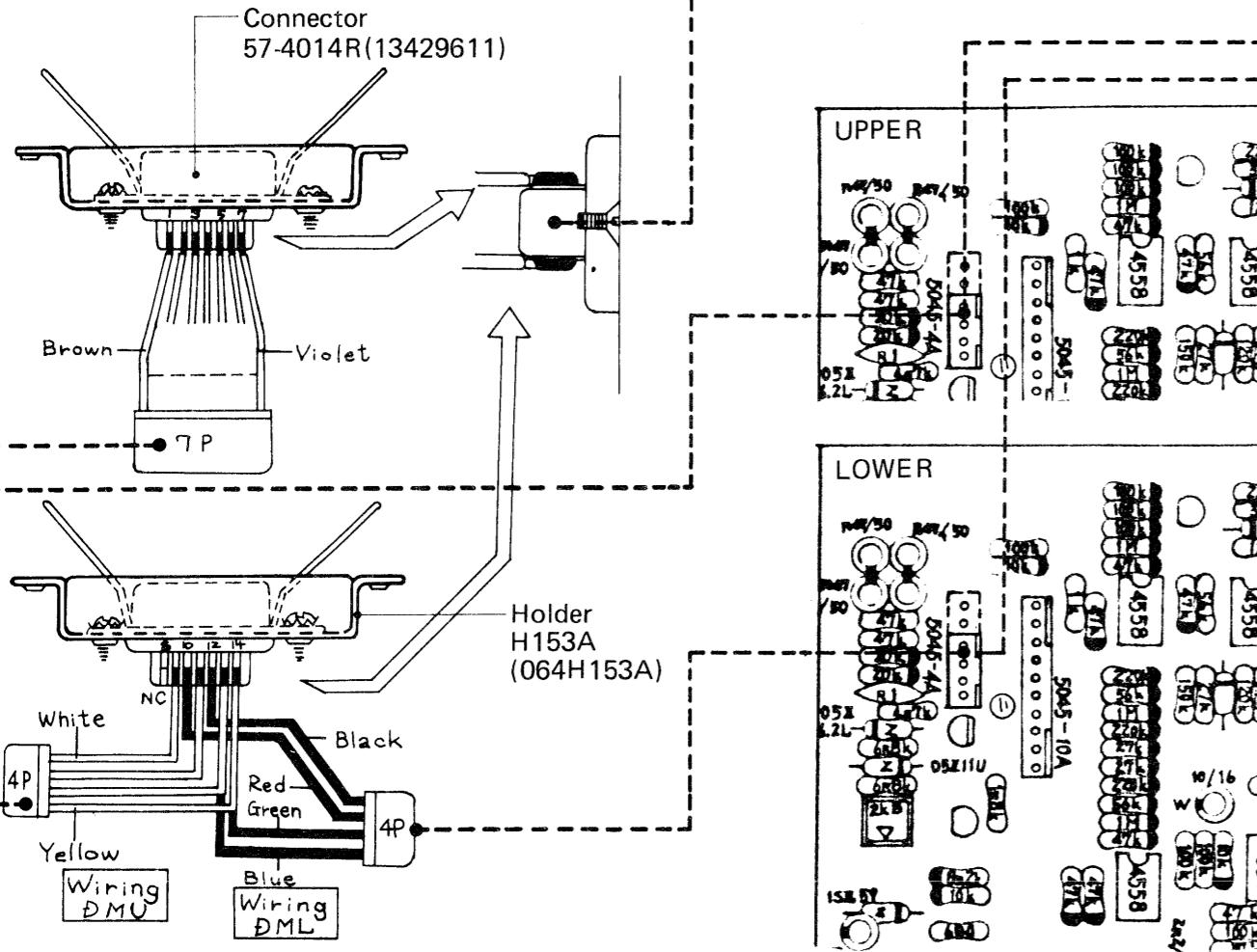
DCB CONNECTOR ASS'Y



DCB PIN ASSIGNMENT

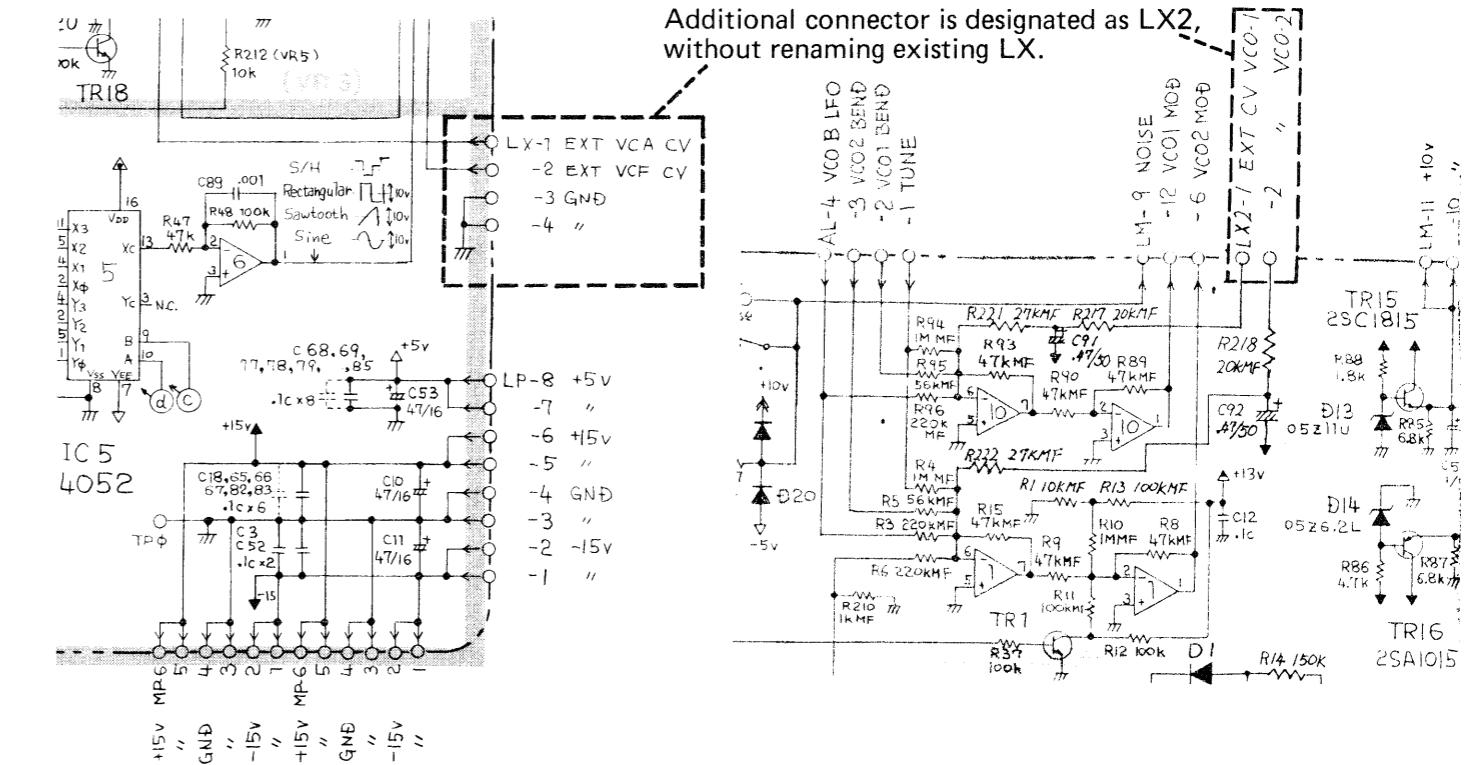
PIN	DESCRIPTION	PIN	DESCRIPTION
1	RX BUSY	8	NC
2	DATA	9	VCA UPPER
3	CLOCK	10	LOWER
4	GND	11	VCF UPPER
5	TX BUSY	12	LOWER
6	DATA	13	VCO-2
7	CLOCK	74	VCO-1

DCB (Digital Communication Bus)



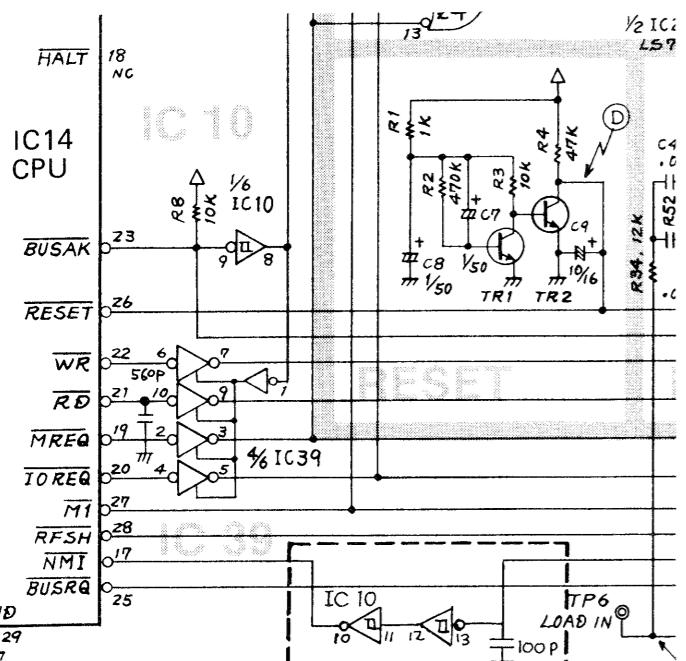
MODULE CONTROLLER BOARD

Additional connector is designated as LX2, without renaming existing LX.

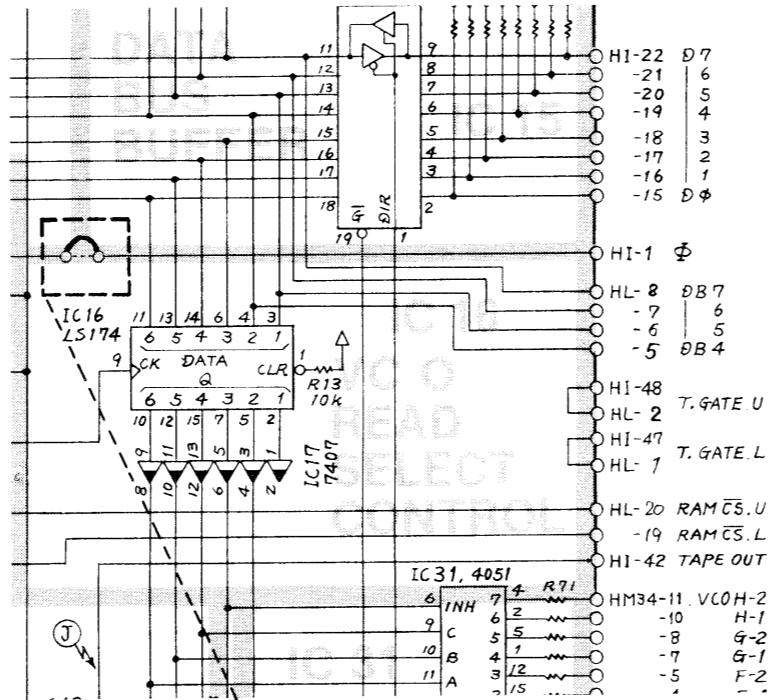
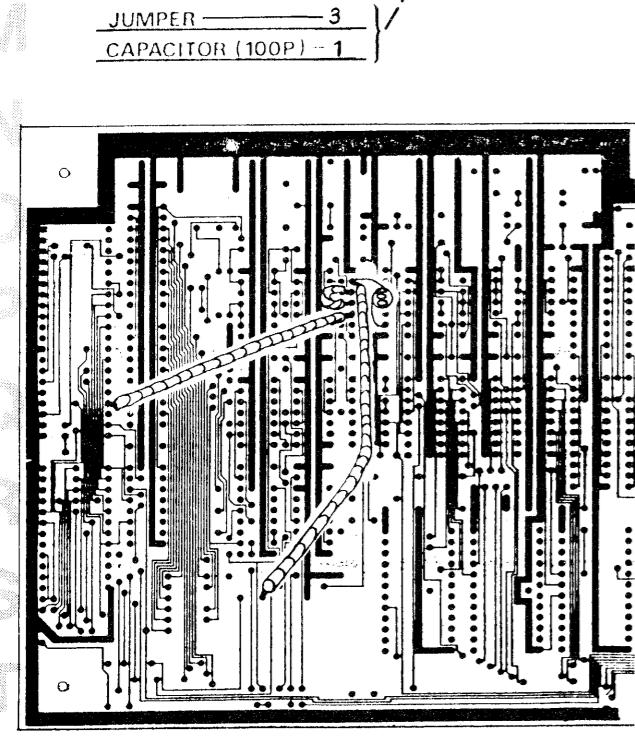


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

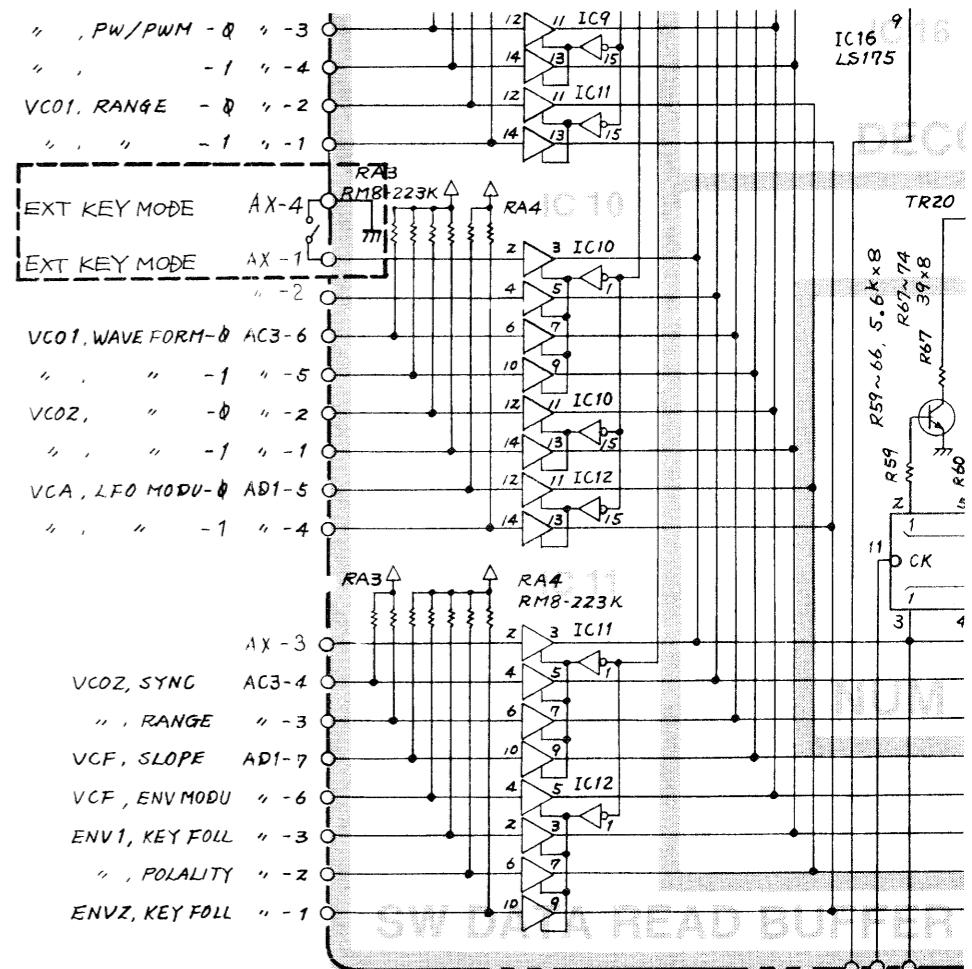
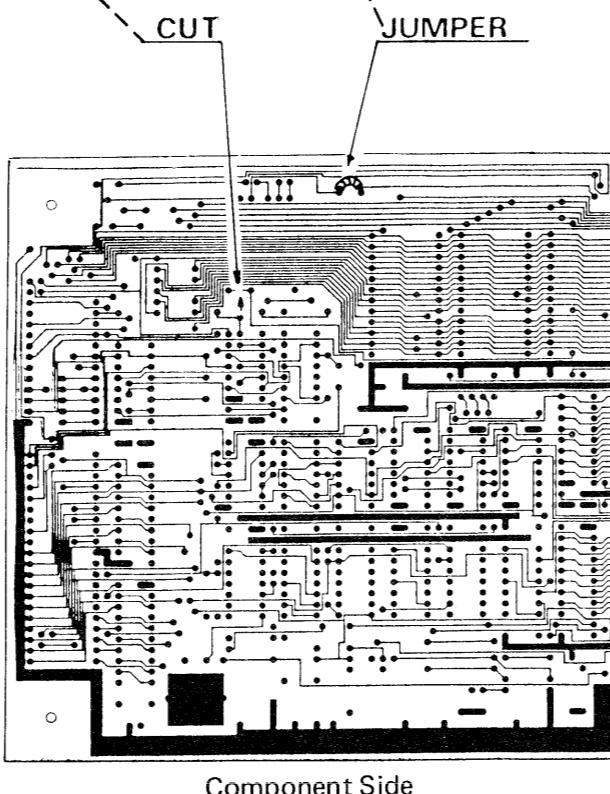
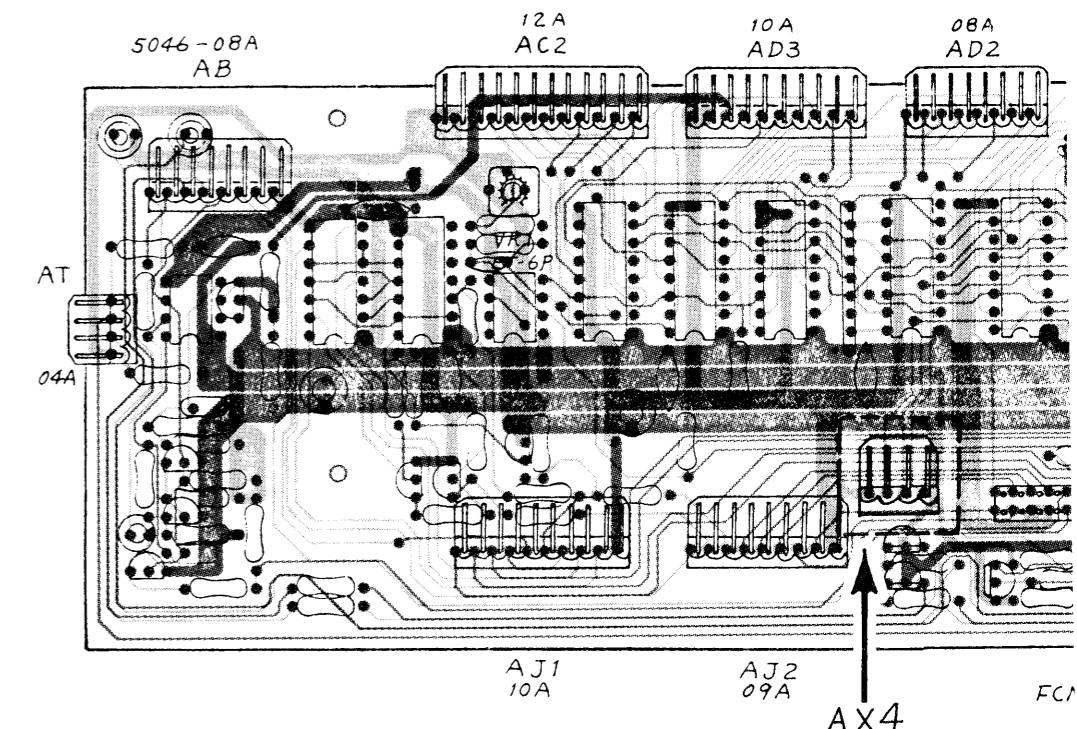
## Circuits Changes related to DCB Board Installation



## CPU BOARD



## PANEL BOARD A



## DIAGNOSTIC PROGRAM IN PROM D

On the CPU board (of JP-8 furnished with the OC-8 or DCB board) located is IC33 (3.3D or 3.4D) which contains not only digital communication program, but also diagnostic program. The program, when executed in the TEST mode, simplifies testing and fault isolation of some of the ICs and their associated circuits listing to the right. For this program to run, the remaining PROMs (IC34-IC36) of CPU board must be of 3.2 version.

### PRECAUTIONS

Allow plenty of time for warm-up (approx. 30 minutes).

If the CPU, PROMs or other circuits fail to perform their basic functions, the program will not start.

### STEPS

1. Turn the JP-8 OFF.
2. To put the JP-8 into the TEST mode, either;
  - a) Turn the power ON while pressing PATCH NUMBER buttons 1 and 3.
  - or
  - b) Set SI-1 and SI-2 of the Interface board to TEST, then turn the power ON.

The test program is executed in the order listed and is stopped wherever it encounters a defective IC (or a problem pertaining to a particular IC), and displays the suspected IC number in the window.

To resume the program, press any touch button. (For example, MANUAL.)

At the end of program, the window displays both the PROM D version and the DAC's bit format, for example;

33 12 -- 3.3D, 12-bit DAC  
34 14 -- 3.4D, 14-bit DAC

IC 35	IC 36	PROM A
IC 35	IC 35	PROM B
IC 34	IC 34	PROM C
IC 33	IC 33	PROM D
① IC 05	IC 6	RAM
② IC 05	IC 5	RAM
IC 20	IC 20	RAM
③ IC 19	IC 19	RAM
IC 04	IC 4	RAM
IC 18	IC 18	RAM
④ dA 00	Module A VCO-1, KCV=0, etc.	
④ dA 01	IC14, IC15	D/A MSB
dA 02	IC14, IC15	D/A B2
dA 03	IC14, IC15	D/A B3
dA 04	IC14, IC15	D/A B4
dA 05	IC14, IC15	D/A B5
dA 05	IC14, IC15	D/A B6
dA 07	IC14, IC15	D/A B7
dA 08	IC14, IC15	D/A B8
dA 09	IC14, IC13	D/A B9
dA 10	IC14, IC13	D/A B10
dA 11	IC14, IC13	D/A B11
dA 12	IC14, IC13	D/A B12
dA 13	IC14, IC13	D/A B13
dA 14	IC14, IC13	D/A LSB

### NOTES FOR TABLE

1. 3.3D doesn't check IC5 and IC6.
2. Because of misprogramming, 3.3D will display these IC numbers in reverse order. If displayed, read; IC20 as IC19, and IC19 as IC20.
3. Output from Module A VCO-1 is applied to the DAC Check. Consequently, if this VCO fails, all the remaining tests will not be performed.
4. Push any button, and the version with 00 is displayed.
5. IC13 and IC15 on the 12-bit interface board are inversely numbered.
6. Read; IC13 as IC15, and IC15 as IC13.
7. If the 13-bit line malfunctions in the 14-bit D/A, the CPU concludes that the D/A is 12-bit, and skips the 13th and 14th bits.

## DESCRIPTION OF CONNECTION CABLES

In the below, SN refers to Serial Number of OP-8.

- For serial numbers up to and including SN220269, the OP-8 was provided with Flat Cable H146 for connecting the OP-8 to the JP-8.

- Effective from serial number SN230270, the OP-8 unit can be connected to the JP-8 through the Flat Cable H146 provided with the OC-8 unit, or to the JUNO-60 through the DCB Cable H165 provided with the OP-8 unit.

- Roland provides not only DCB Cable H165 but also DCB Cable H172 for interconnecting JP-8 or JUNO-60 as shown here.

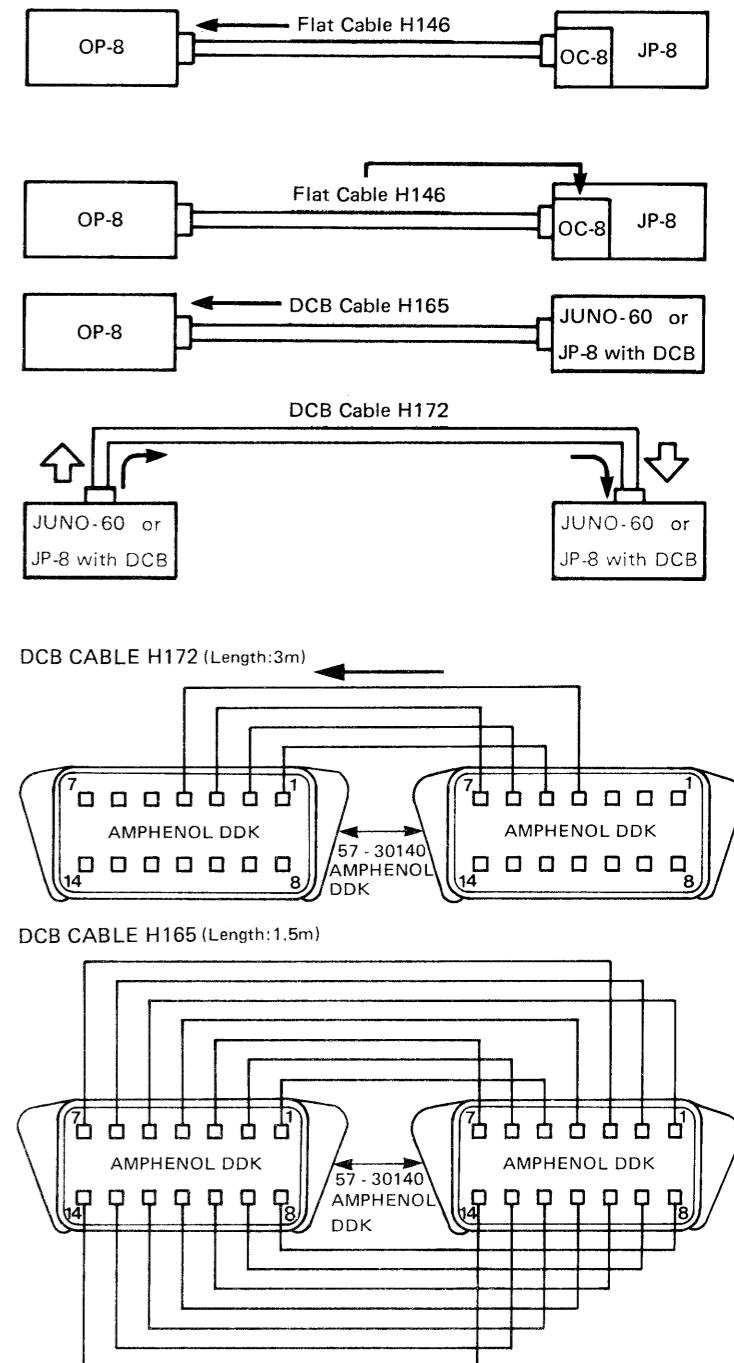
- DCB Cable H172 is uni-directional, with the signal-flow direction shown by the arrow on the connector.

When connecting two JUNO-60 or JP-8 units, be sure to connect the cable so that the arrow points away from the JUNO-60 or JP-8 unit to be played, and towards the JUNO-60 or JP-8 unit to be controlled.

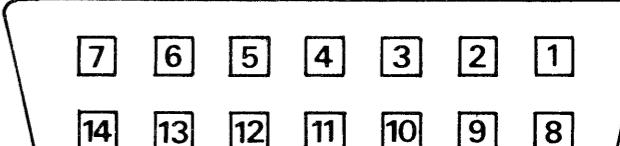
Also, when controlling the JUNO-60 with the OP-8, DCB Cable H172 can be used to connect the OP-8 to the JUNO-60.

Be sure to connect the cable so that the arrow points away from the OP-8 and towards the JUNO-60. Otherwise, the JUNO-60 may operate incorrectly.

On the other hand, DCB Cable H165 is a bi-directional cable in which sent from the TX-terminal on a unit returns to the RX-terminal on the unit, causing regeneration.



### DCB Pin Configurations



(View from Rear Panel)

## PARTS LIST CHANGE

PART. SERIAL NO.	FROM	TO	PART NO.
<b>INTERFACE BOARD</b>			
<b>SN 171700</b> PCB Ass'y PCB D/A Converter (IC14) Latches	OPH122 052H268 Am6012 LS273 LS175 LS175 IC25, IC26 IC22 IC9 <b>SN 212330</b> IC9	OPH122A 052H268 ITS80141 TC40H273 (IC15, CMOS) TC40H174 (IC13, CMOS) TC40H175 (IC11, CMOS) HD14051 (CMOS) (Hitachi only) TC4001 4013BP (CMOS) TC40H74P	149H122A 15219127 15159507 15159511 15159512 15159113H0 15159101T0 15159105T1 15159510 ICs: ALL INCOMPATIBLE
<b>CPU BOARD</b>			
<b>SN 171700</b> IC34-IC36	$\mu$ PD2716 (version 1.0)	$\mu$ PD2716-JP8-A (IC36) $\mu$ PD2716-JP8-B (IC35) $\mu$ PD2716-JP8-C (IC34)	15179609 (version 3.x) 15179610 (version 3.x) 15179611 (version 3.x) (version 3.x = 3.1 or 3.2)
<b>MODULE CONTROLLER BOARD</b>			
<b>SN 202100</b> PCB Ass'y PCB IC3 Ladder Resistor TRs, 11, 12, 25 TR26 Switches	OPH123 052H269 TL082 Discrete R601611 (RA6) 2SA1015 2SC1815 .....	OPH123A 052H269 BA662A R601611 (RA6) 2SA798-G (TR11) 2SA798-G (TR25) SSB212 (SWs 1, 2)	149H123A 15229802 15119108 15119108 13159123
<b>SN 202210</b> IC49 RAM	2101 only	2101 or 5101 (Compatible with minor modification. See pp. 37, 38.)	15179303
<b>PANEL BOARD F</b>			
<b>LED (display)</b> <b>SN 242750</b>	LN526RA	LN5260A	15029409  (Compatible but different in brightness and color; mix use should be avoided.)
<b>PANEL BOARD E</b>			
<b>PANEL BOARD G</b>			
<b>SN 272850</b> Switches (LEDs)	KHC11901 (AR3432S)	KHC11026 (SEL2210R)	13169610  (Switch proper remains unchanged. The new LED has better off-axis luminous density. Mix use should be avoided.)

## SN 282880-UP JP-8 WITH DCB BOARD

PART NAME	FROM	TO	PART NO.
Top Panel Chassis (jack) Holder (rear)	Panel H78B Chassis H116 .....	Panel H78C Chassis H116A Holder H184	072H078C 061H116A 064H184
<b>DCB BOARD</b>			
PCB Ass'y Holder IC1 IC3 Flat Cable	.....	OPH220 Holder H185 74LS21 $\mu$ PD8251AC Flat Cable H126 (INTFCE-CPU)	149H220 (pcb 052H380B) 064H185 15169350 15179112 053H213
DCB Connector Holder Slide Switch	.....	57-40140R Holder H153 SSB-022-12RN	13429611 064H153 13159118
<b>CPU BOARD</b>			
IC33	.....	$\mu$ PD2716-JP8-D	15179612 (version 3.4)

In order to expedite delivery of products or because of procurement problem, the factory is occasionally forced to make minor substitution of ICs.

Such substitutions will work satisfactorily and compatible with the initial IC unless otherwise noted in related sections (circuit diagram, parts list, etc.).

## PART NUMBER

Usually, equivalent semiconductors are assigned to the same part number as initial component with two-letter suffix identifying the manufacturer. For example, TO - Toshiba, ZO - Motorola.

In ordering such ICs, uncertain suffix can be omitted from the part number, and the factory will supply suitable ones with notes or cautions, as necessary.

Parts on the PARTS LIST	Equivalent
TC4052BP	HD14052BP
TC4051BP	HD14051BP
TC40175BP	$\mu$ PD4175BC
$\mu$ PD2101ALC	M5L2101AP-4 $\mu$ PD5101LC M5L5101LP-1
$\mu$ PD780C-1	LH0080A
$\mu$ PD2716D	M5L2716K MB8516
$\mu$ PD444C	M58981P-45
$\mu$ PD2114C	M5L2114LP
$\mu$ PD8253C	M5L8253P-5
TL082CP	NJM082DR $\mu$ PC4082C
74LS Series	M74LS series
74.. Series (exp. 7406)	M532.. series M53206)

## APPENDIX

## PCB EDITION

Dot and circle above PCB code are indicative of edition; "●" stands for 1, and "○" for 5. Example: ○● = 6th edition.

Illustrated on pp. 48-50 is information on MODULE and MODULE CONRTROLLER Boards mounted on the JP-8 models with serial numbers up to 090599. For circuit diagram, refer to p.11 or p.12 although some small discrepancies may exist.

## CAUTION ON REPLACEMENT OF PCBs IN THIS SECTION

Although terminal for terminal compatible, when mix used, new and old PCBs process signals in slightly different way, reproducing voices that are distinguishable form each other. Therefore, when replacing MODULE or MOD CON board in this section, use a set of PCBs of the same edition group as described below.

NOTE: Replacement of MODULE board can be made independently of MOD CON board, and vice versa.

## MODULE CONTROLLER BOARD

group A

○● 052H269 or ○● 052H269

## MODULE BOAD

group B

○● 052H269-up ○● 052H270-up

When replacements for MOD CON are of group B, check IC49 (RAM) for name.

If it is 5101, see p.38 for necessary modification.

Listing below are descriptions of surface mounting, jumper wire, and conductive foil cut made on the MOD COM boards up to the abovementioned serial numbers, shown on the next page.

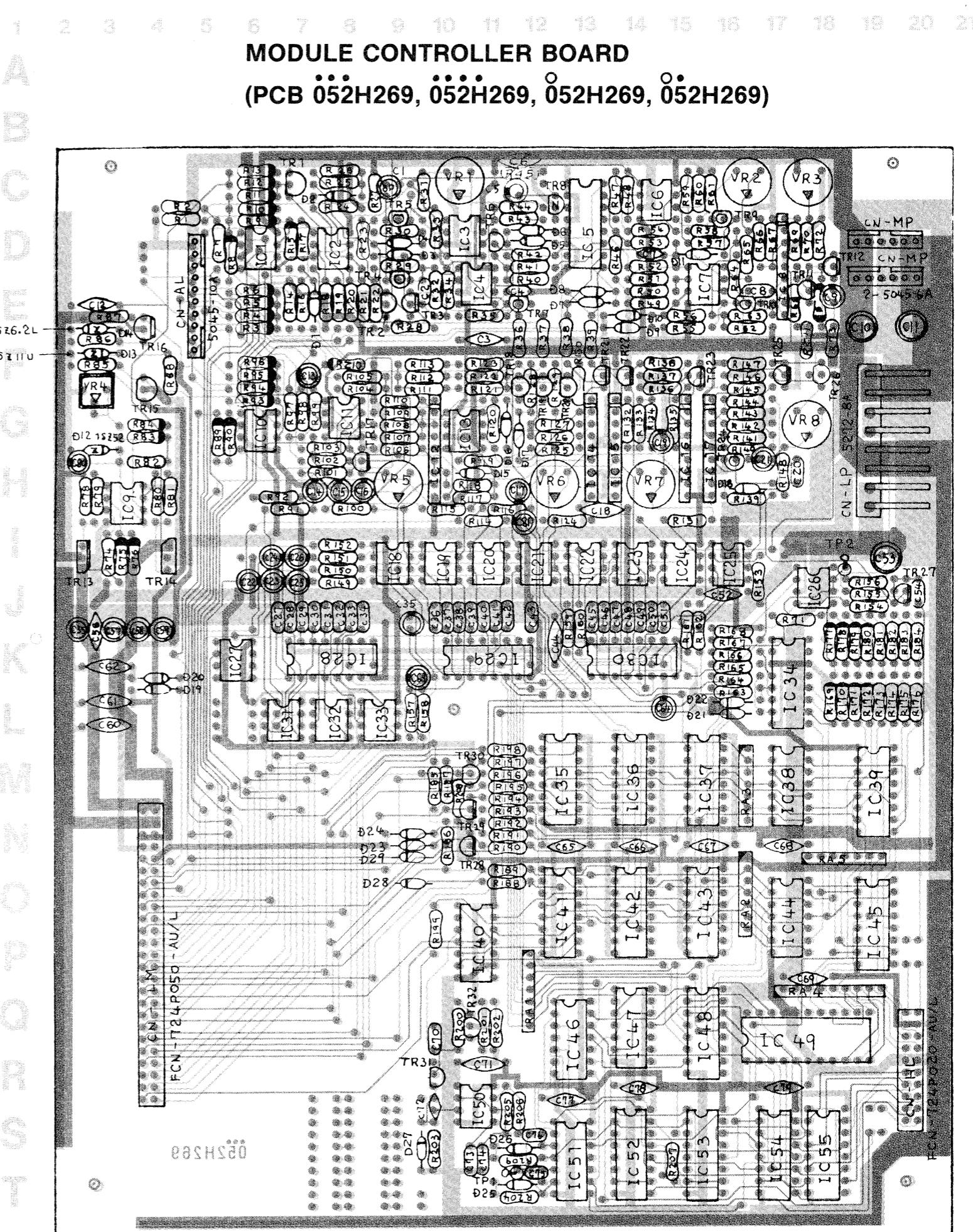
## ABBREVIATIONS

C-pattern cut Di-diode R-resistor J-jumper M-mylar cap

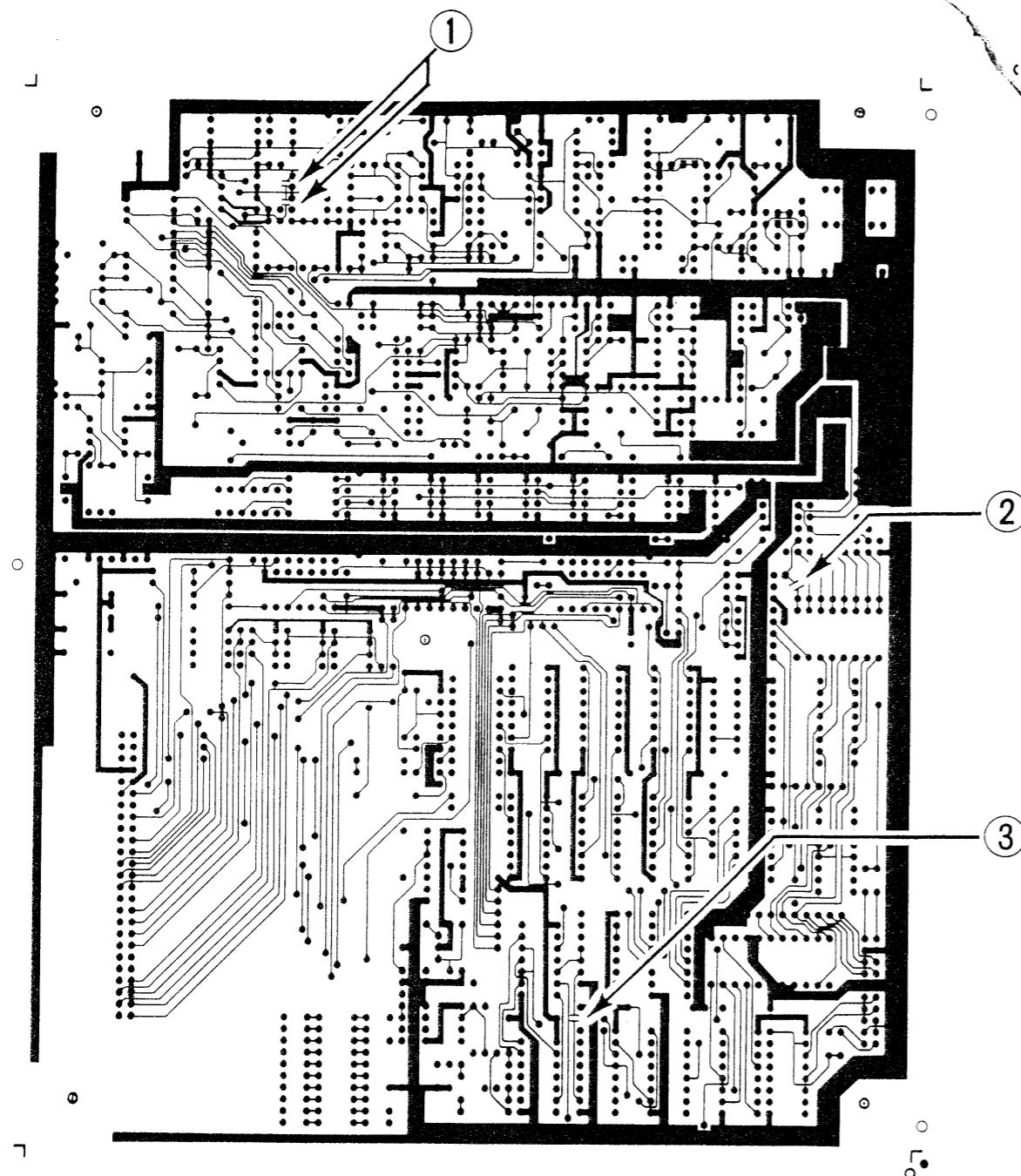
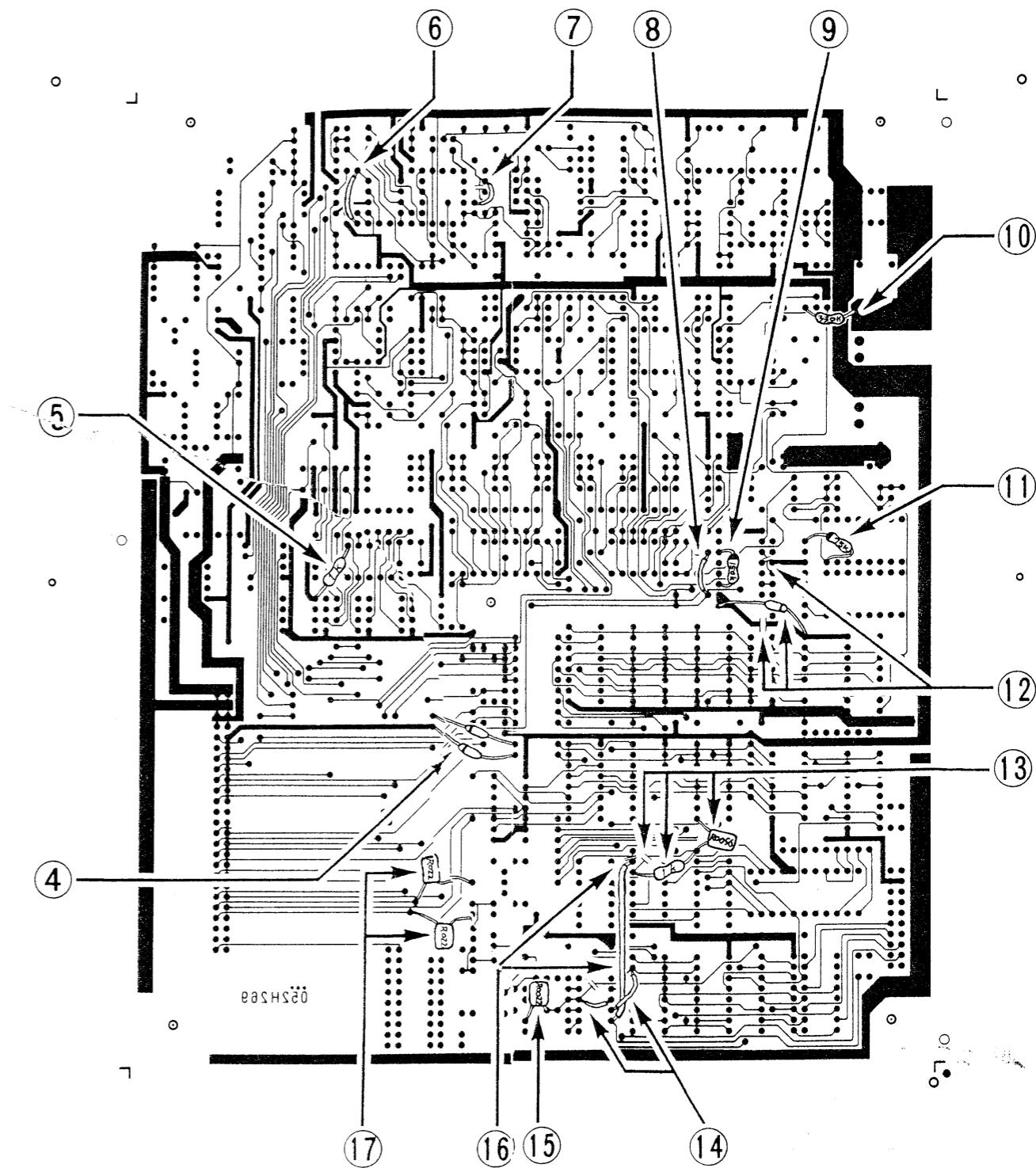
Serial numbers

1B-050199 2A-050200 2B-060299 3A-060300 4A-070400 5A-080500 5B-090599

No.	Part	SN	No.	Part	SN
1	C	up to 2B	10	R	5A-up
2	C	3A-5B	11	R	3A-5B
3	C				
4	D	up to 1B	12	D 2xC	3A-5B
5	R	3A-5B	13	M.R.C	2A-up
6	J	up to 2B	14	J.C	4A-5B
7	J.C	4A-5B	15	M	4A-5B
8	J	5A-up	16	J.C	2A-5B
9	R	up to 2B	17	M	3A-5B



## PATTERN-CUTS ON MOD CON

PATTERN-CUTS & SURFACE-MOUNTINGS  
ON MOD CON

## MODULE BOARD OPH124

SN 030100-090599 (pcb 052H270 or 052H270)

